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Intel® Media Center Reference Platform

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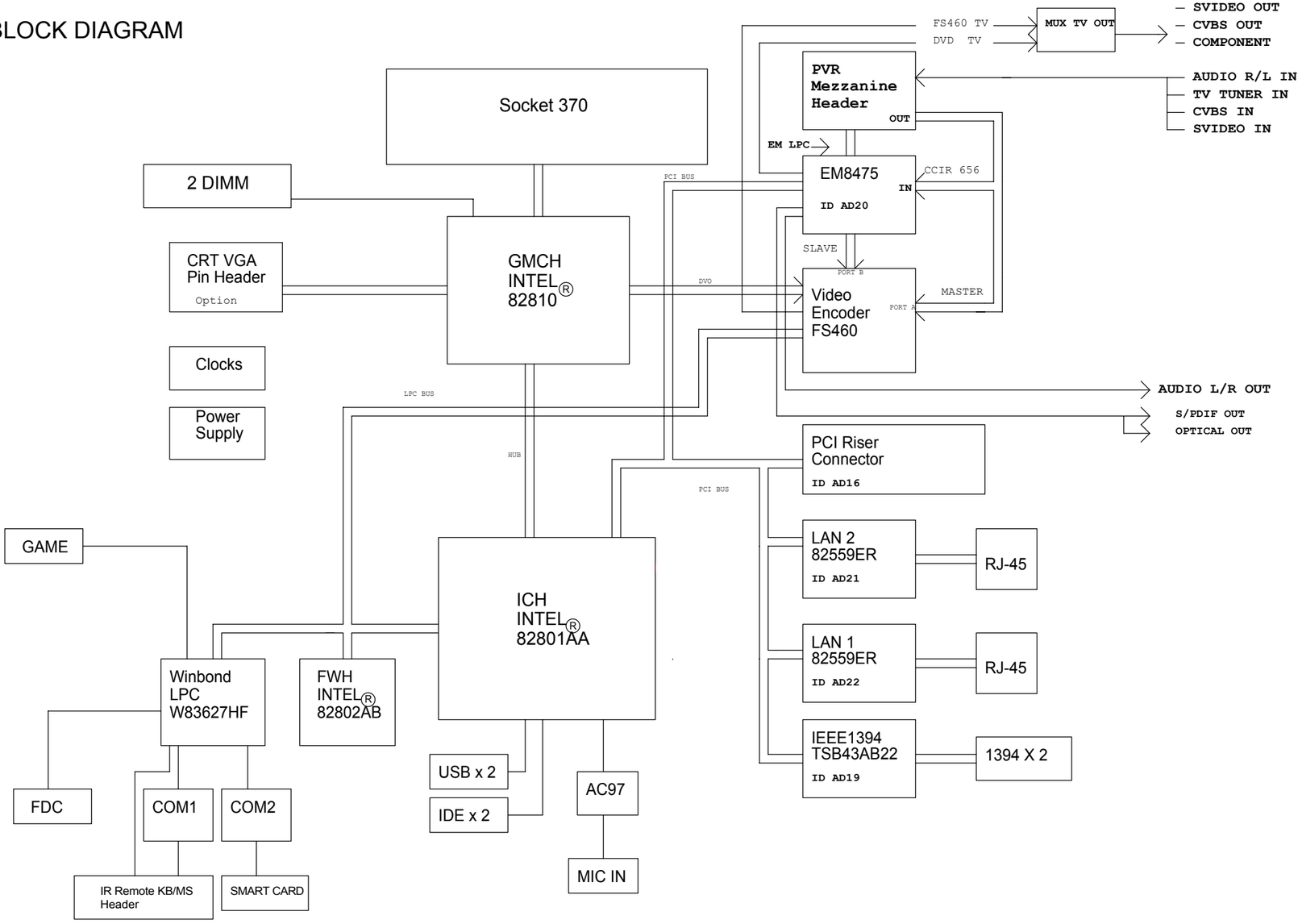
BLOCK DIAGRAM



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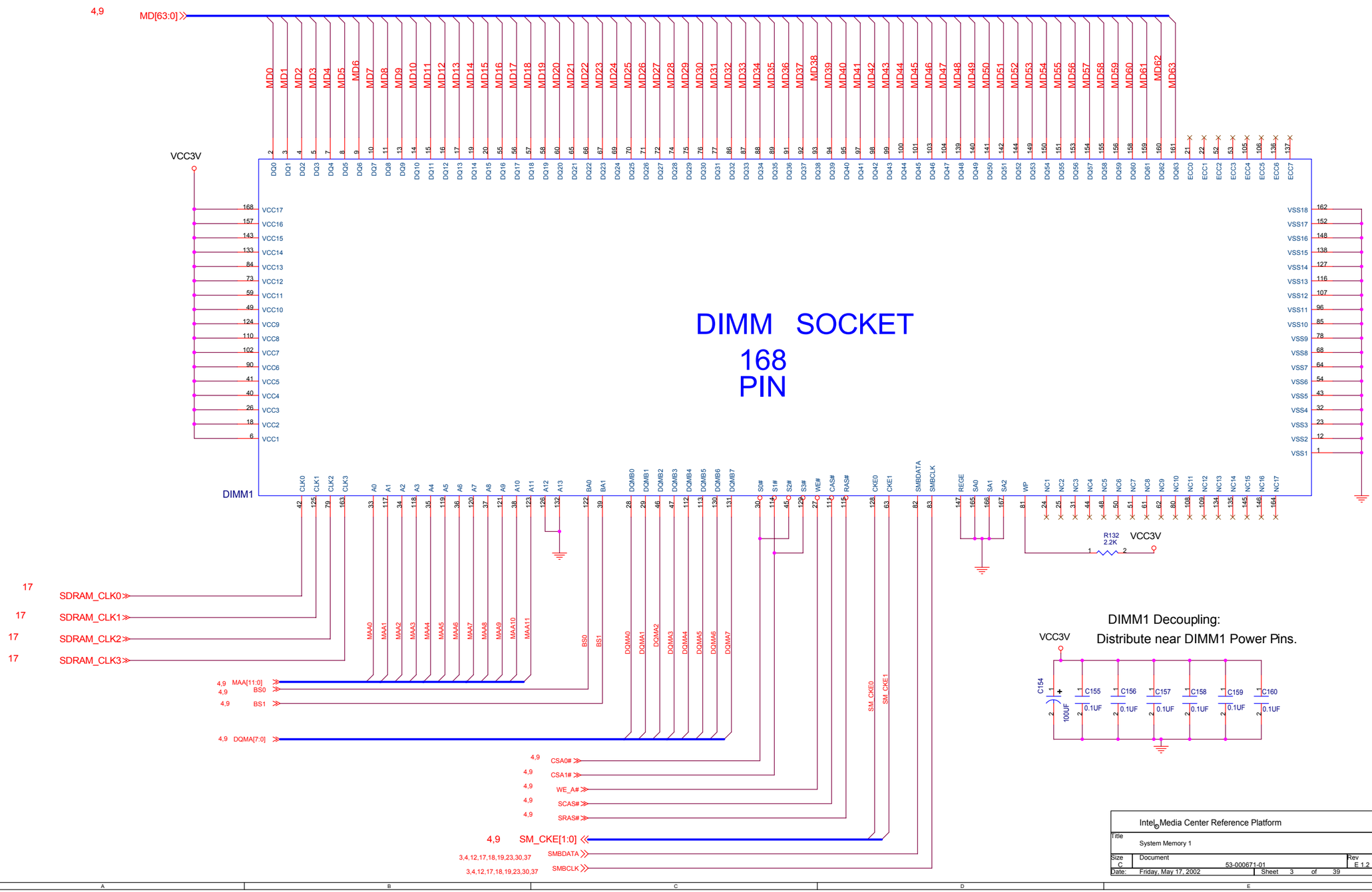
System Memory 1



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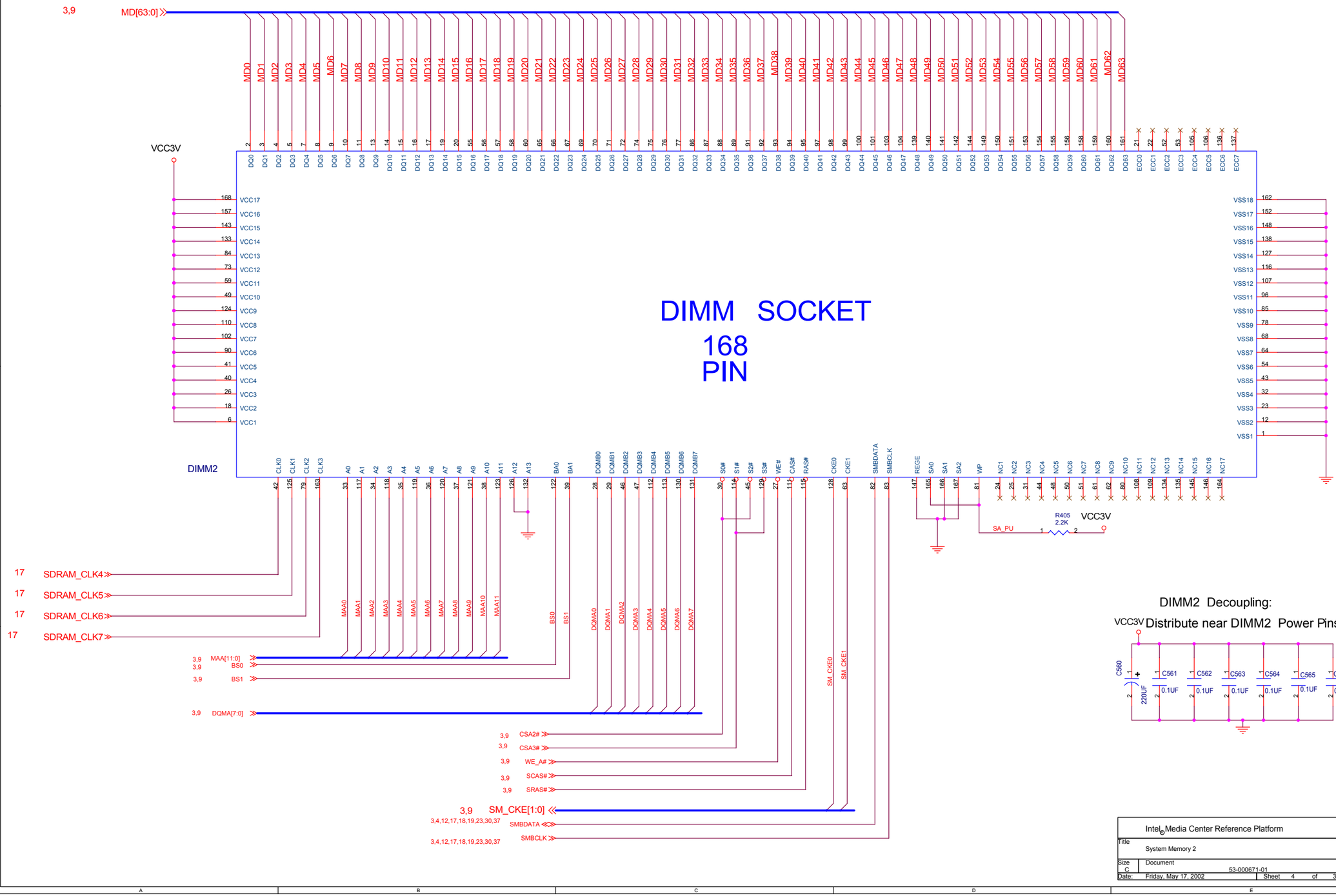
System Memory 2



DIMM2 Decoupling:

VCC3V Distribute near DIMM2 Power Pins.

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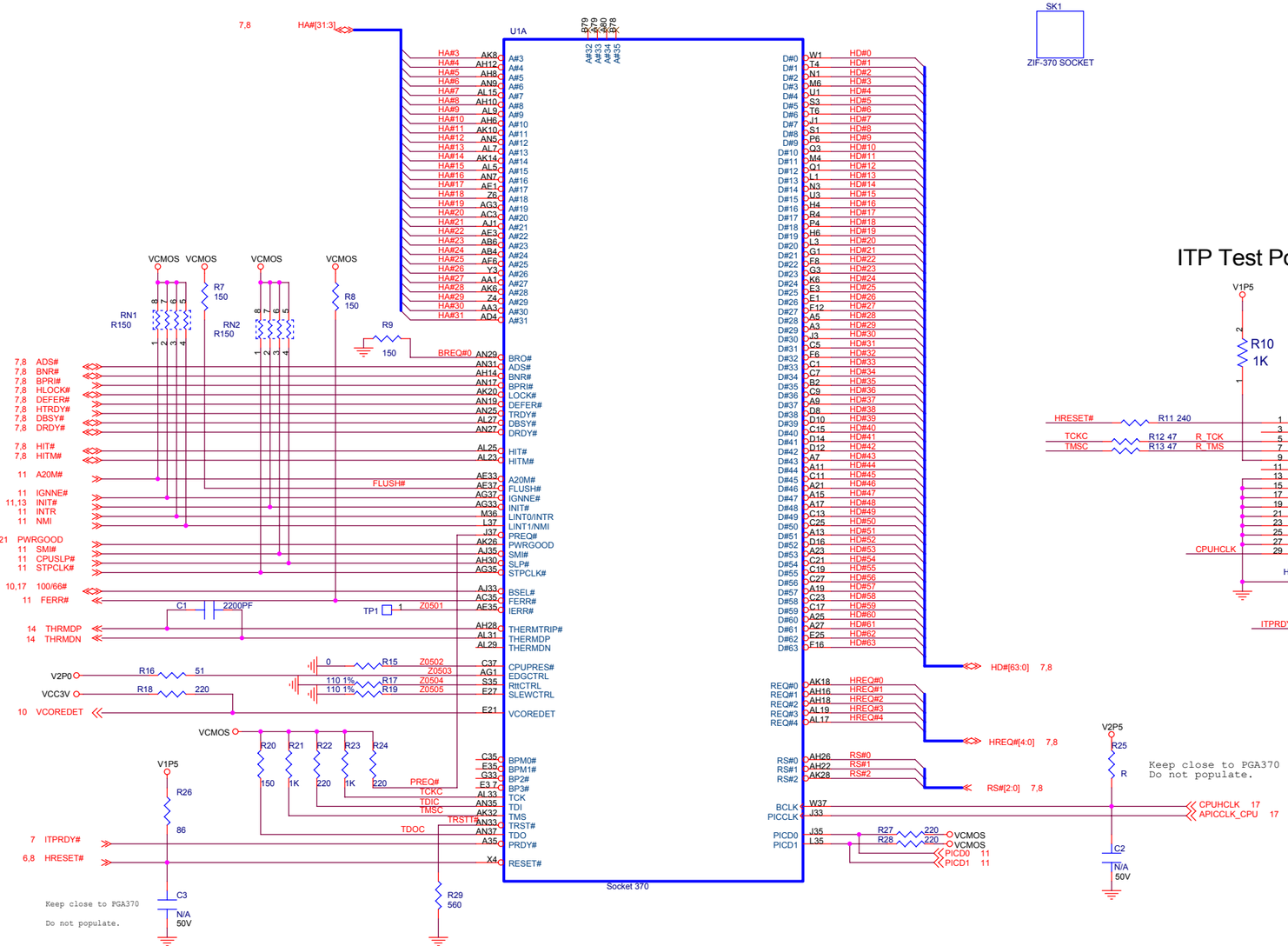

Intel® Media Center Reference Platform			
Title: CPU Part 1			
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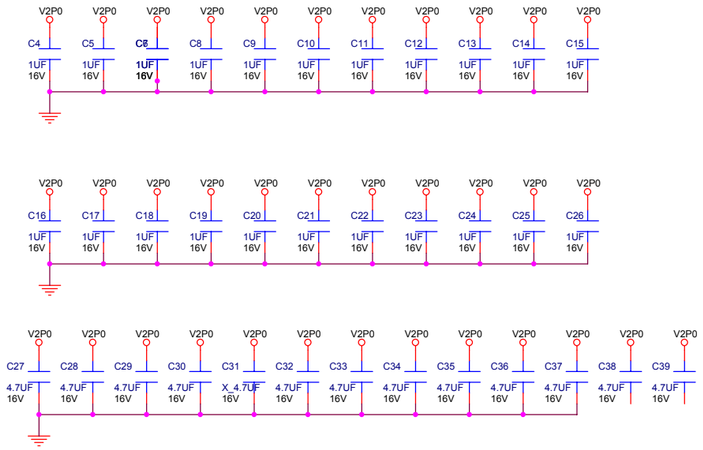

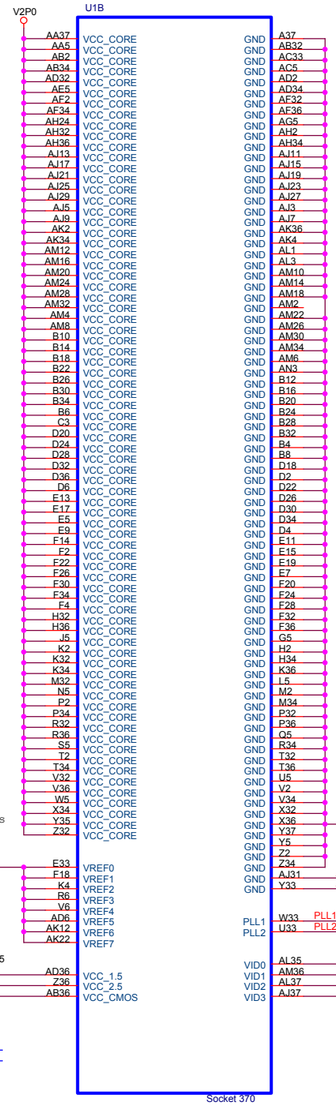

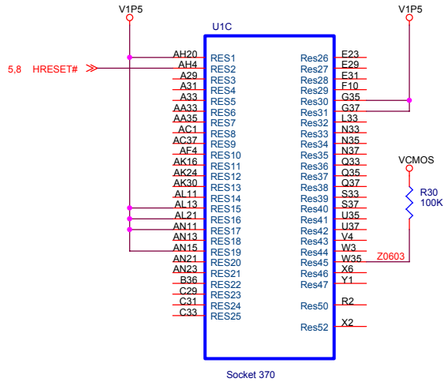

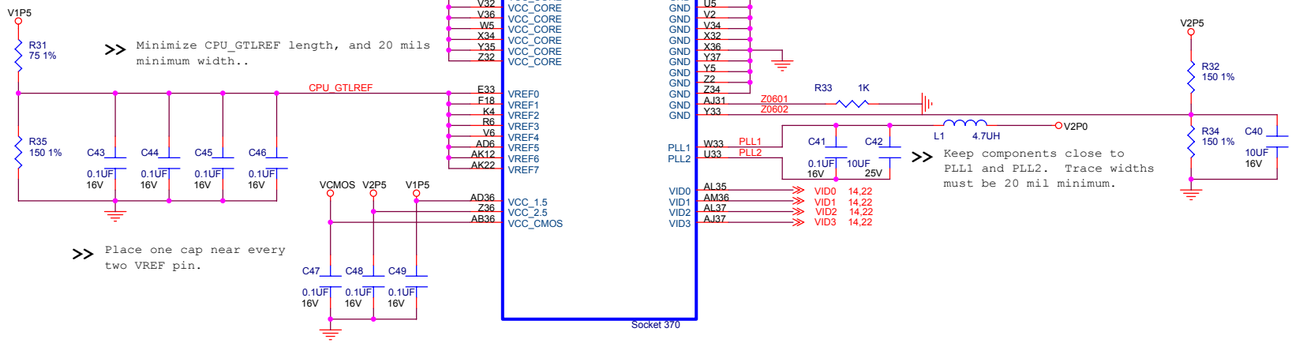

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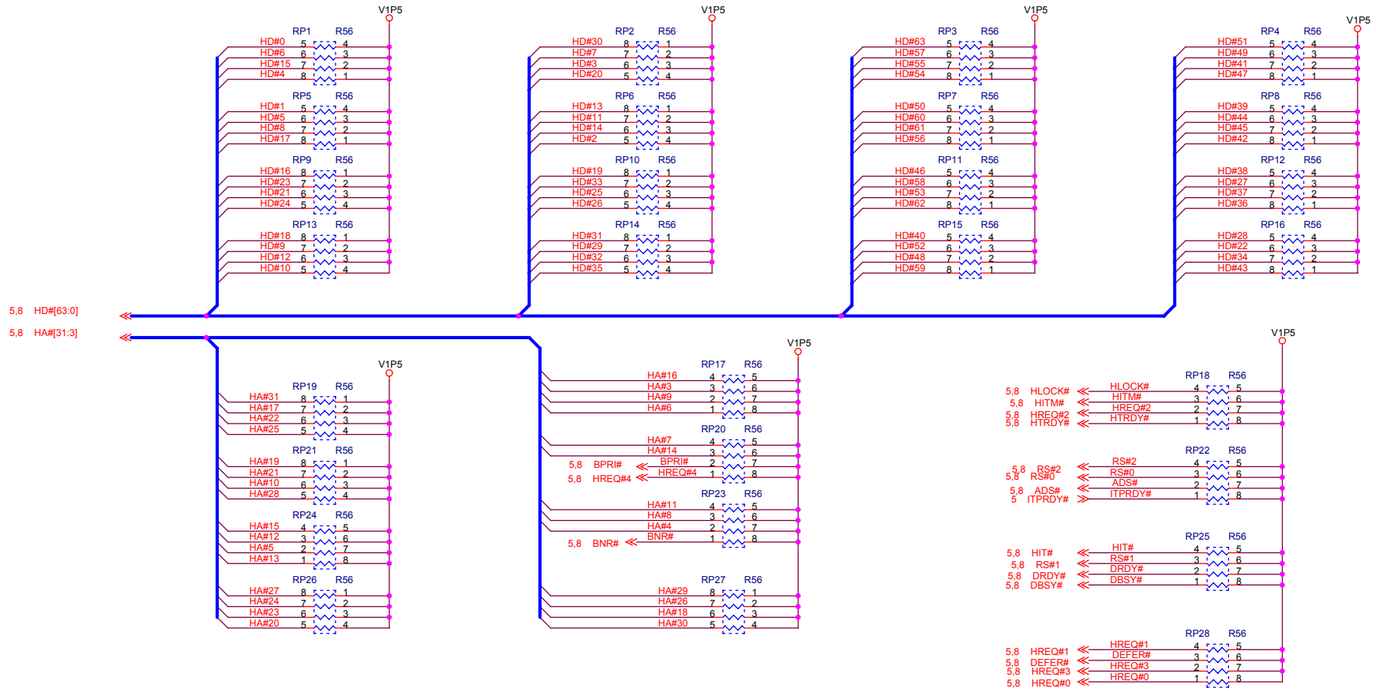
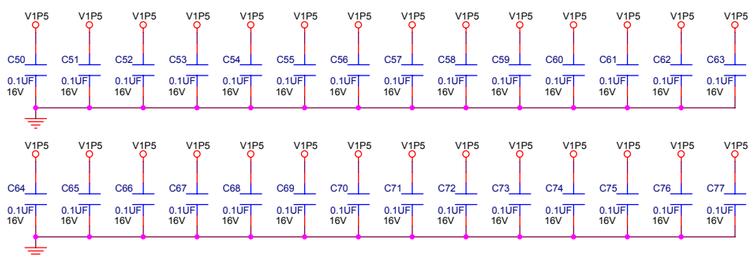
GTL+ TERMINATION RESISTORS



>> Place one CAP for every resistor pack.



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Title: GTL+ Termination		
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82810 PART 1: Host Interface

V1P5

R36
75 1%

R38
150 1%

C78 0.1UF 16V

C79 0.01UF 16V

C80 1UF 16V

GMCHGTLREF

V2P5

R37
R

Do not Stuff

Place site w/in 0.5" of clock ball (V6)

C81 N/A 16V

17 GMCHHCLK
8,11,13,14,15,18,19,20,24,28,32,35,37

V1P8

B20 VCC1_8[0]
P6 VCC1_8[1]
U18 VCC1_8[2]

V17 VCC_CORE[0]
V16 VCC_CORE[1]
V15 VCC_CORE[2]
V14 VCC_CORE[3]
V10 VCC_CORE[4]
V9 VCC_CORE[5]
V8 VCC_CORE[6]
V7 VCC_CORE[7]
F17 VCC_CORE[8]
F16 VCC_CORE[9]
F14 VCC_CORE[10]
F10 VCC_CORE[11]
F8 VCC_CORE[12]
F7 VCC_CORE[13]

M5 GTLREFA
W13 GTLREFB

V6 HTCLK
M2 RESETB
AB4 CPURST#
P5 HLOCK#
R3 DEFER#
N3 ADS#
T3 BNR#
T1 BPRI#
M4 DBSY#
N1 DRDY#
P1 HIT#
R1 HITM#
N4 HTRDY#

PCIRST#
5,6 HRESET#
5,7 HLOCK#
5,7 DEFER#
5,7 ADS#
5,7 BNR#
5,7 BPRI#
5,7 DBSY#
5,7 DRDY#
5,7 HIT#
5,7 HITM#
5,7 HTRDY#

5,7 HA#[31:3]

U5 HA3# — HA#3
U1 HA4# — HA#4
V4 HA5# — HA#5
V1 HA6# — HA#6
T4 HA7# — HA#7
U2 HA8# — HA#8
U3 HA9# — HA#9
W1 HA10# — HA#10
U4 HA11# — HA#11
W3 HA12# — HA#12
W4 HA13# — HA#13
T5 HA14# — HA#14
W2 HA15# — HA#15
V2 HA16# — HA#16
AC2 HA17# — HA#17
AA2 HA18# — HA#18
Y3 HA19# — HA#19
AB3 HA20# — HA#20
AA1 HA21# — HA#21
AB2 HA22# — HA#22
AC3 HA23# — HA#23
AA3 HA24# — HA#24
Y2 HA25# — HA#25
AB5 HA26# — HA#26
AC4 HA27# — HA#27
Y1 HA28# — HA#28
AC5 HA29# — HA#29
Y4 HA30# — HA#30
AB1 HA31# — HA#31

5,7 HREQ#[4:0]

R4 HREQ0# — HREQ#0
T2 HREQ1# — HREQ#1
P4 HREQ2# — HREQ#2
R2 HREQ3# — HREQ#3
R5 HREQ4# — HREQ#4

5,7 RS#[2:0]

N5 RS0# — RS#0
P2 RS1# — RS#1
N2 RS2# — RS#2

Y22 VSS[0]
V18 VSS[1]
N22 VSS[2]
J22 VSS[3]
Y19 VSS[4]
C19 VSS[5]
E22 VSS[6]
K14 VSS[7]
K13 VSS[8]
K12 VSS[9]
K11 VSS[10]
K10 VSS[11]
L14 VSS[12]
L13 VSS[13]
L12 VSS[14]
L11 VSS[15]
L10 VSS[16]
M14 VSS[17]
M13 VSS[18]
M12 VSS[19]
M11 VSS[20]
M10 VSS[21]
N14 VSS[22]
N13 VSS[23]

82810

U2A

HD0# Y5 — HD#0
HD1# W5 — HD#1
HD2# W8 — HD#2
HD3# AA6 — HD#3
HD4# AB6 — HD#4
HD5# Y6 — HD#5
HD6# AA5 — HD#6
HD7# AA9 — HD#7
HD8# V5 — HD#8
HD9# AC7 — HD#9
HD10# AB7 — HD#10
HD11# AC8 — HD#11
HD12# AA7 — HD#12
HD13# Y8 — HD#13
HD14# W7 — HD#14
HD15# AC6 — HD#15
HD16# W9 — HD#16
HD17# AC9 — HD#17
HD18# Y7 — HD#18
HD19# AA10 — HD#19
HD20# AB8 — HD#20
HD21# AC10 — HD#21
HD22# AB13 — HD#22
HD23# AB10 — HD#23
HD24# AB9 — HD#24
HD25# AB11 — HD#25
HD26# Y10 — HD#26
HD27# AB16 — HD#27
HD28# AB12 — HD#28
HD29# Y11 — HD#29
HD30# Y9 — HD#30
HD31# AC12 — HD#31
HD32# W11 — HD#32
HD33# AC11 — HD#33
HD34# W12 — HD#34
HD35# AA11 — HD#35
HD36# AA13 — HD#36
HD37# Y13 — HD#37
HD38# Y12 — HD#38
HD39# AC14 — HD#39
HD40# AA15 — HD#40
HD41# AC15 — HD#41
HD42# Y14 — HD#42
HD43# AC13 — HD#43
HD44# AA14 — HD#44
HD45# AB14 — HD#45
HD46# Y17 — HD#46
HD47# Y15 — HD#47
HD48# AC17 — HD#48
HD49# AC16 — HD#49
HD50# AA18 — HD#50
HD51# AB15 — HD#51
HD52# W15 — HD#52
HD53# AB18 — HD#53
HD54# W17 — HD#54
HD55# AA17 — HD#55
HD56# W18 — HD#56
HD57# W16 — HD#57
HD58# AC19 — HD#58
HD59# Y16 — HD#59
HD60# AB19 — HD#60
HD61# Y18 — HD#61
HD62# AC18 — HD#62
HD63# AB17 — HD#63

HD#[63:0] 5,7

INTEL 82810 (GMCH)

PART1

HOST INTERFACE

V1P8

C82 10UF 16V
C83 0.1UF 16V
C84 0.1UF 16V
C85 0.1UF 16V
C86 0.1UF 16V
C87 0.1UF 16V
C88 0.01UF 16V
C89 0.01UF 16V

GMCH Core Plane Decoupling:

Place 1 .1uF/.01uF pair in each corner, and 2 on opposite sides close to component if they fit.

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82810 PART 2 : System Memory & HUB Interface

INTEL 82810 (GMCH)®

PART 2

SYSTEM MEMORY

AND

HUB INTERFACE

HUB I/F

U2B

82810

Place HUBREF Generation Circuit in middle of GMCH and ICH.

Place C102 as close as possible to GMCH

Place Resistor as Close as possible to GMCH

Intel® Media Center Reference Platform			
Title	82810 Part 2 : System Memory & HUB Interface		
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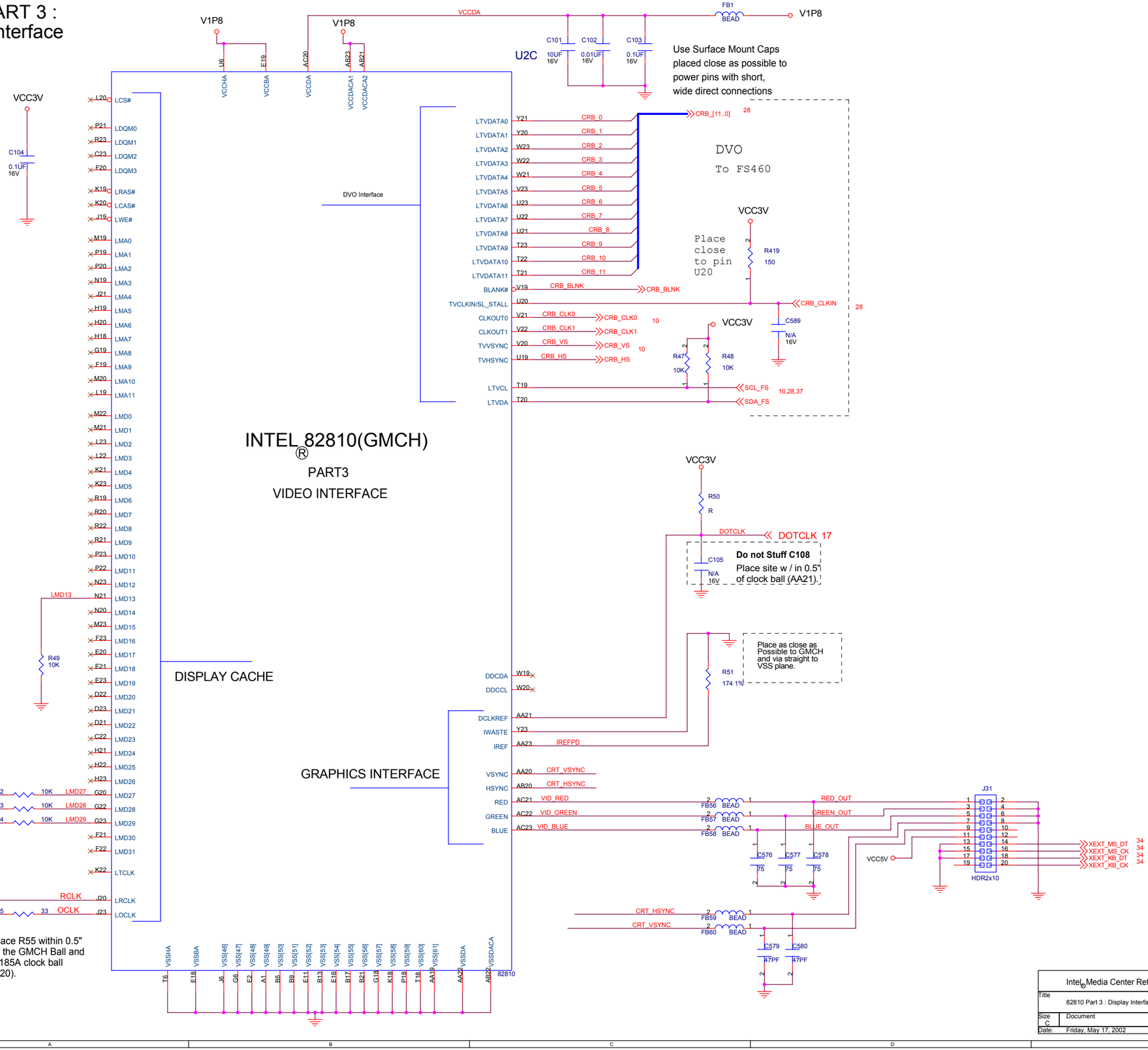
82810 PART 3 : Display Interface



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Title: 82810 Part 3 : Display Interface		
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82801AA (ICH)
Part 1

INTEL 82801AA (ICH)®

PART 1

VCC3V

V1P8

U3A

82801AA(ICH)

CPU

HUB I/F

PCI

PC/PCI

18,19,20 AD[31:0]

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

11,18,19,20,24,32 C/BE#[3:0]

C/BE#0 C/BE#1 C/BE#2 C/BE#3

17 PCLK_ICH

18,19,20,24,32 FRAME#
18,19,20,24,32 DEVSEL#
18,19,20,24,32 IRDY#
18,19,20,24,32 TRDY#
18,19,20,24,32 STOP#
8,11,13,14,15,18,19,20,24,28,32,35,37 PCIRST#
18,19,20,24,32 LOCK#
18,19,20,24,32 PAR
18,19,20,24,32 SERR#
11,18,19,20 PCI_PME#

SLOT # 4 20 REQ4#
20 GNT4#
20,32 REQ5#
SLOT # 5 20,32 GNT5#

A20M# 5 CPUSLP# 5 FERR# 5 IGNNE# 5 INIT# 5,13 INTR 5 NMI 5 SMI# 5 STPCLK# 5 RCIN# 14 A20GATE 14

HL[10:0] 9

HLSTB 9 HLSTB# 9 IHCOMP_PU HUBREF 9

INTA# 20,24 INTB# 19,20 INTC# 20 INTD# 20

IRQ14 15 IRQ15 15 APICCLK_ICH 17 PICD1 5 PICD0 5 SERIRQ 14,28

REQ0# 20 REQ1# 20 REQ2# 18,20 REQ3# 19,20

GNT0# 20 GNT1# 20 GNT2# 18,20 GNT3# 19,20

RESV2

For Test/Debug
Don't Stuff R122

Place R189 as close as possible to ICH0.

Place C172 as close as possible to ICH0.

VCC3V R57 R

C121 N/A 16V

R61 8.2K A20GATE
R62 8.2K RCIN#
R63 8.2K SERIRQ

R56 40 1%

C120 0.1UF 16V

R58 8.2K
R59 8.2K

R60 R

C107 C108 C109 C110 C111 C112 C113 C114 0.1UF 16V / 0.01UF 16V

C115 C116 C117 C118 C119 0.1UF 16V / 10UF 16V

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Title: 82801AA (ICH) Part 1		
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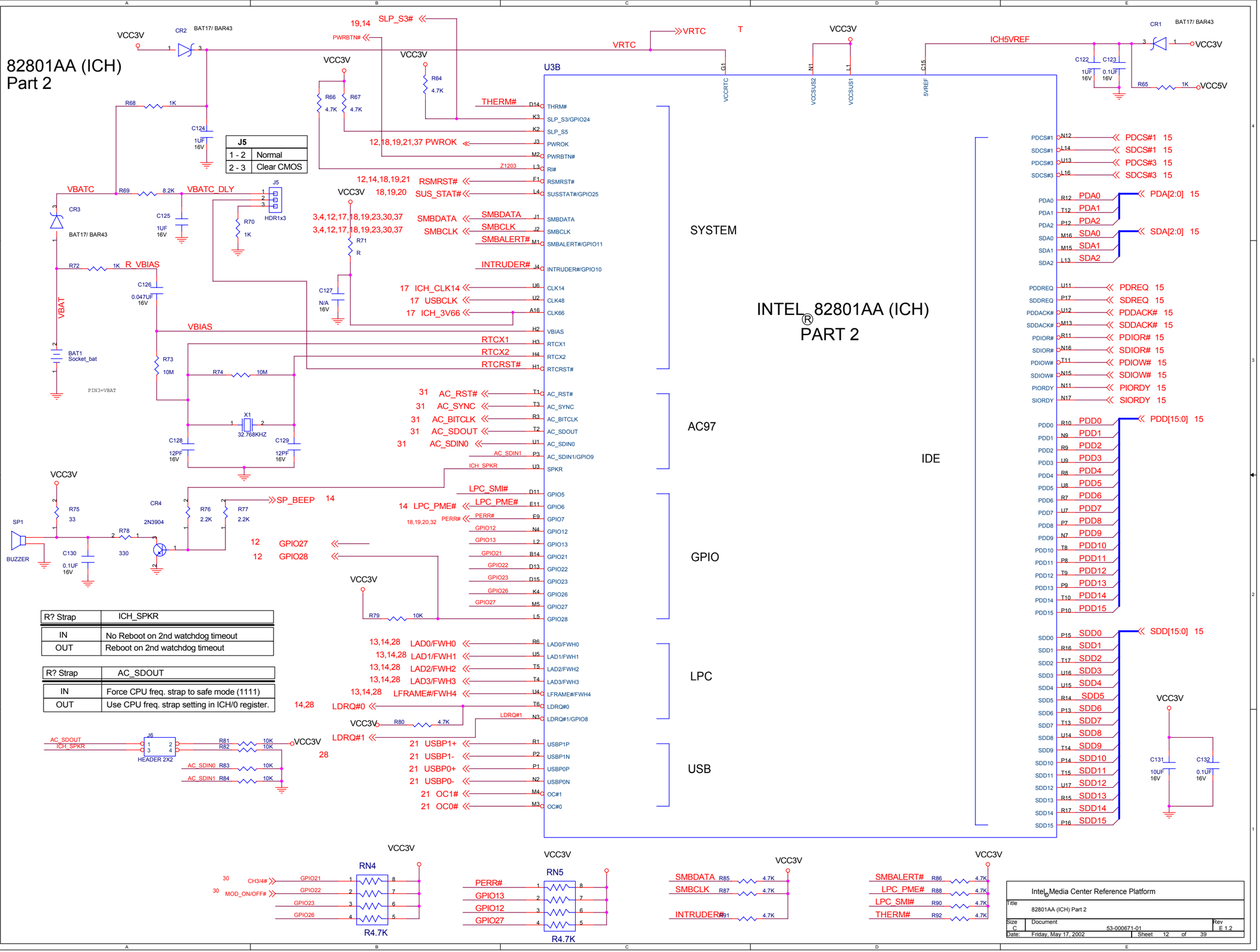
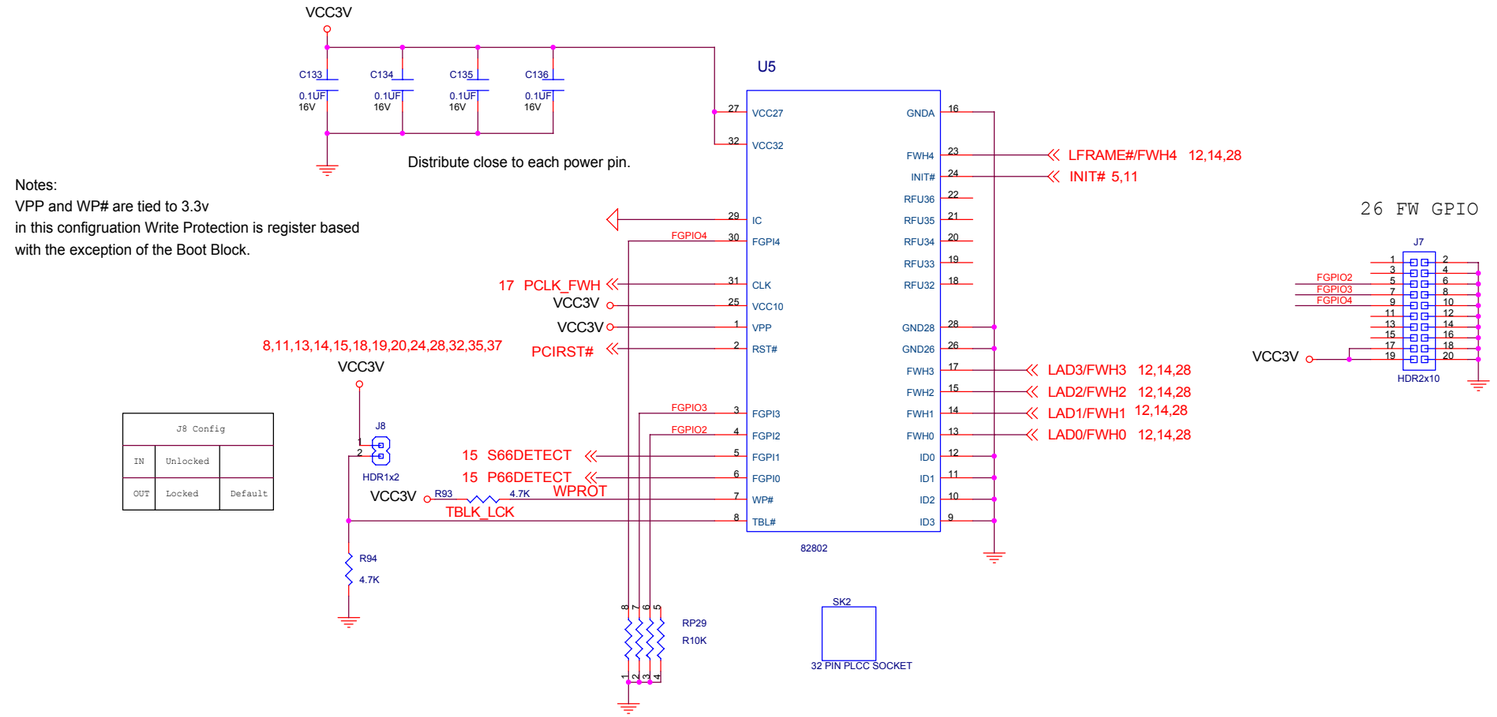
82801AA (ICH) Part 2



Firmware Hub (FWH)



Notes:
VPP and WP# are tied to 3.3v
in this configruation Write Protection is register based
with the exception of the Boot Block.

J8 Config		
IN	Unlocked	
OUT	Locked	Default

Intel® Media Center Reference Platform		
Title: Firmware Hub (FWH)		
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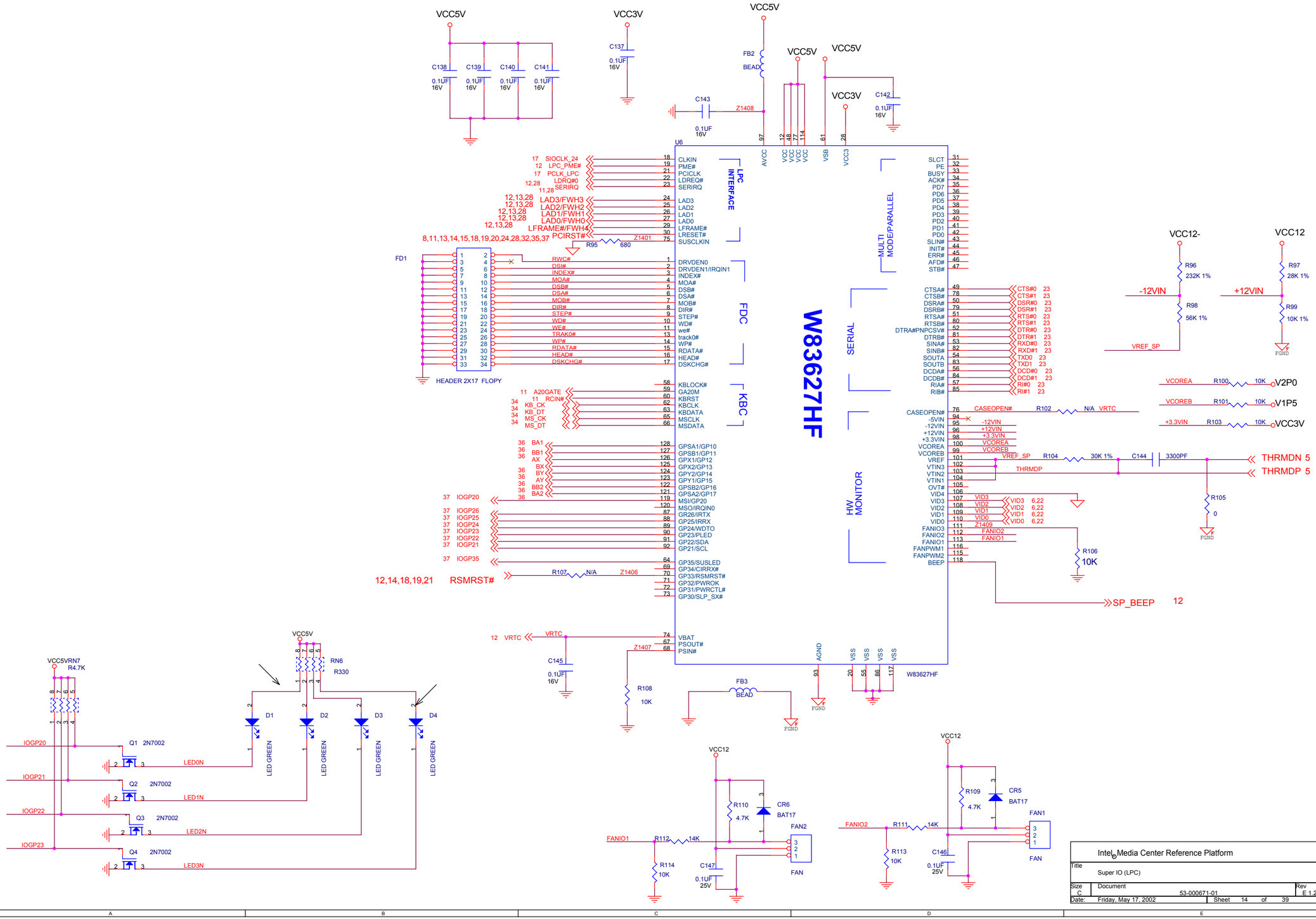
Super IO (LPC)



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Title	Super IO (LPC)
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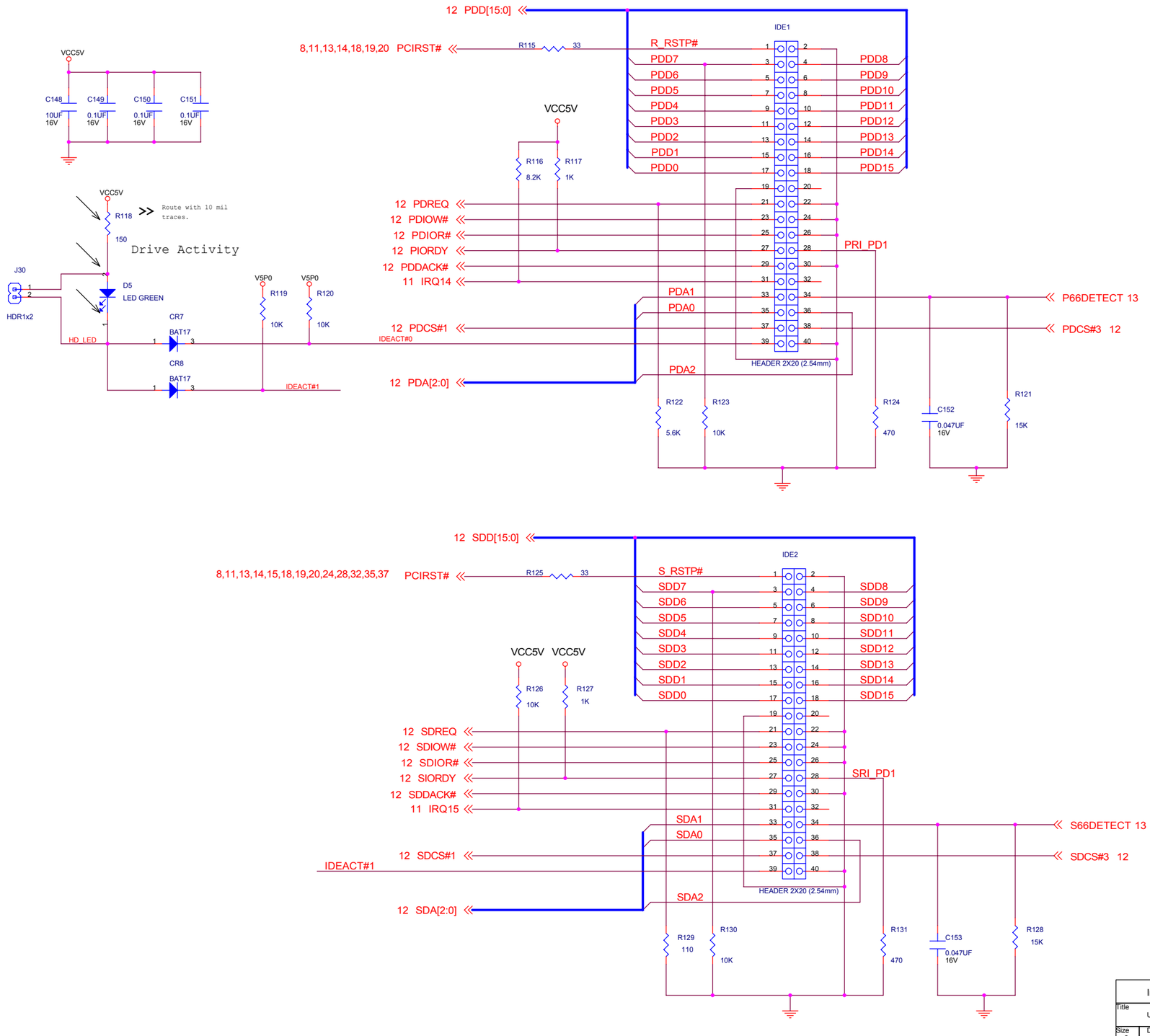
Ultra ATA33/66 IDE Connectors



Intel Media Center Reference Platform		
Title: Ultra ATA33/66 IDE Connectors		
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Intentionally Left Blank

Intel® Media Center Reference Platform			
Title: Intentionally Left Blank			
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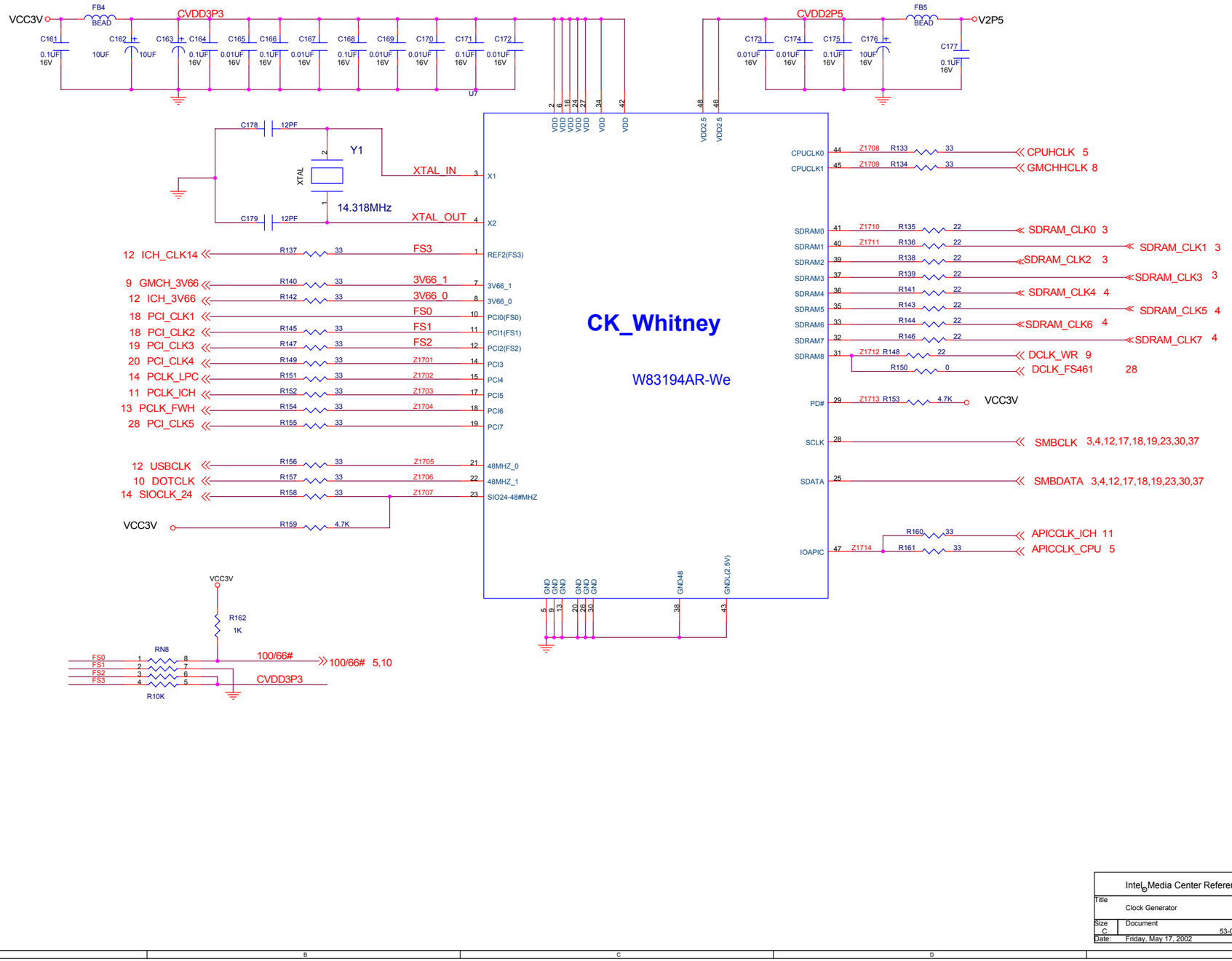
Clock Generator



Intel Media Center Reference Platform			
Title: Clock Generator			
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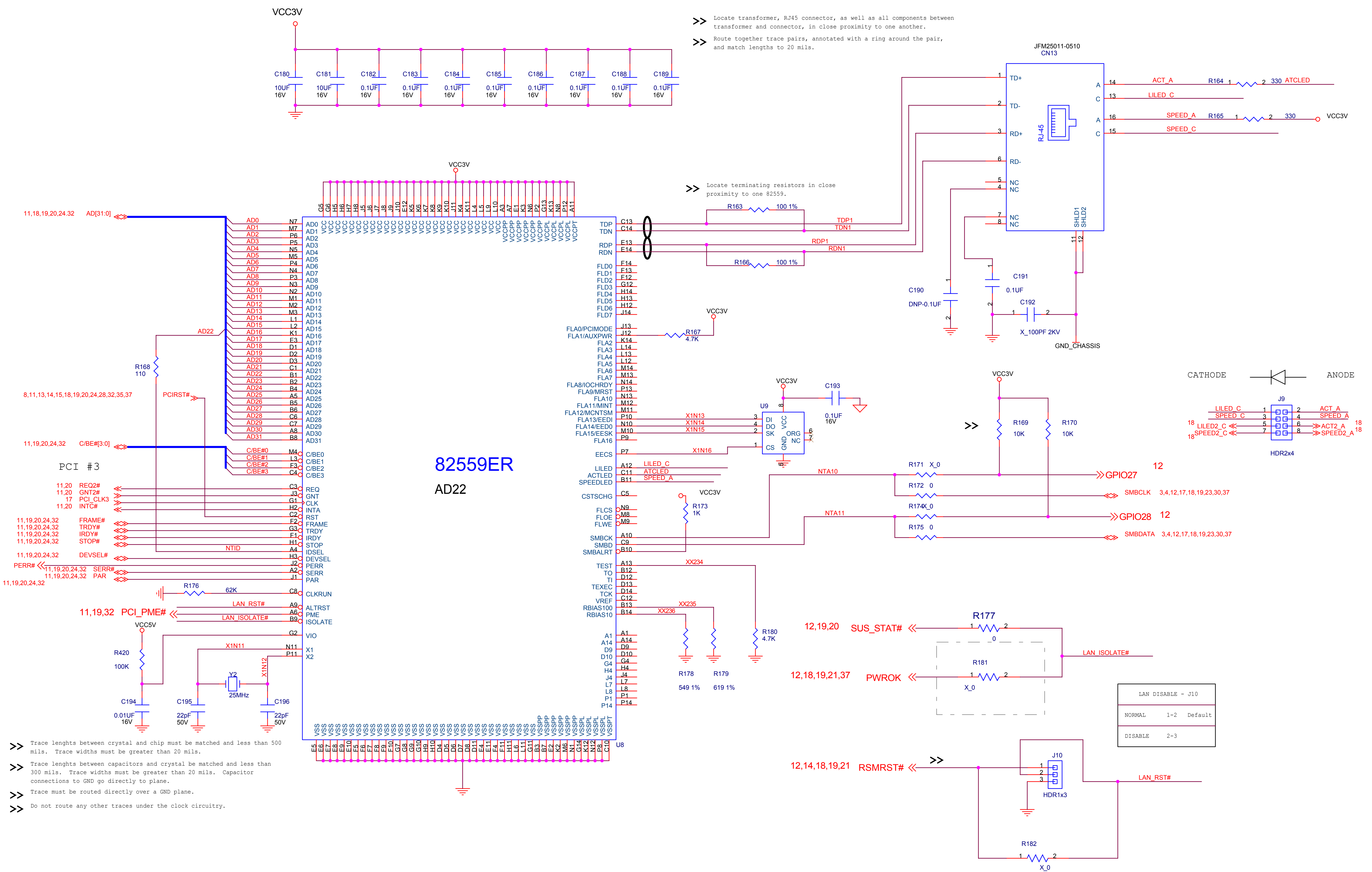
Ethernet Port 1



>> Locate transformer, RJ45 connector, as well as all components between transformer and connector, in close proximity to one another.

>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.

>> Locate terminating resistors in close proximity to one 82559.

>> Trace lenghts between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.

>> Trace lenghts between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.

>> Trace must be routed directly over a GND plane.

>> Do not route any other traces under the clock circuitry.

LAN DISABLE - J10		
NORMAL	1-2	Default
DISABLE	2-3	

SMBus address is determined by serial EPROM.

Intel® Media Center Reference Platform

Title: Ethernet Port 1

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Ethernet Port 2

>> Locate transformer, RJ45 connector, as well as all components between transformer and connector, in close proximity to one another.

>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.

THIS HEADER FOR RJ45 EXTERNAL

DO NOT STUFF

NETWORK LED #2

>> Locate terminating resistors in close proximity to one 82559.

82559ER

AD21

PCI #2

>> Trace lenghts between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.

>> Trace lenghts between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.

>> Trace must be routed directly over a GND plane.

>> Do not route any other traces under the clock circuitry.

SMBus address is determined by serial EPROM.

LAN DISABLE - J12		
NORMAL	1-2	Default
DISABLE	2-3	

Intel® Media Center Reference Platform

Title	Ethernet Port 2		
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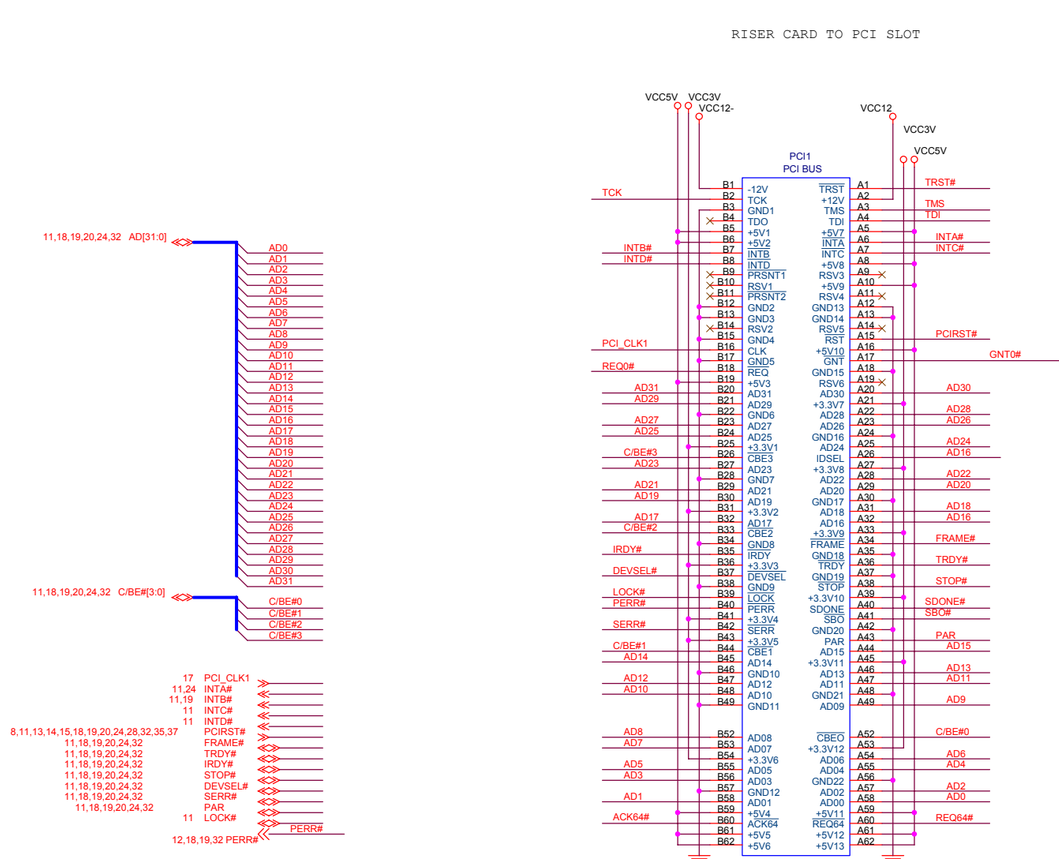
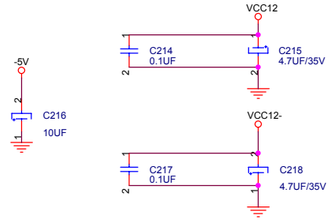
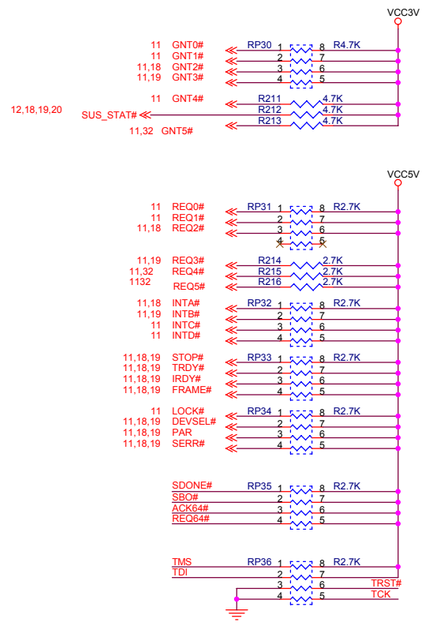
PCI Slot



RISER CARD TO PCI SLOT



PCI Pullups



PCI SLOT	REQ	GNT	INT	ID	CLK	
0	0	0	A	AD16	1	RISER CARD
1	1	1	B	AD21	2	LAN2
2	2	2	C	AD22	3	LAN1
3	3	3	A	AD20	4	EM8475
4	4	4	A	AD17		NO DEVICE
5	5	5	B	AD19	6	1394

Intel Media Center Reference Platform

Title	PCI Slot		
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Power Good Circuit

Resume Reset Circuitry

Schmitt Trigger Logic
using a 22msec delay

Route with traces capable of supporting 1500mA.

Route with traces capable of supporting 1500mA.

SN74LVC06A is 5V output tolerance

Intel® Media Center Reference Platform	
Title	Reset & USB ATX Connector Reset
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Power

VCC5V
RP43
R10K NO
6,14 VID0
6,14 VID1
6,14 VID2
6,14 VID3

VCC3V
C294 C295 C296 C297 C298 C299 C300 C301 C302 C303 0.1UF 16V

VCC3V
C314 C315 C316 C317 C318 C319 C320 C321 C322 0.1UF 16V

VCC12
C304 C305 C306 C307 C308 0.1UF 16V

VCC12-
C309 C310 C311 0.1UF 16V

VCC5V
C312 C313 10UF 16V

VCC3V
C283 C284 C285 C286 C287 C288 C289 C290 C291 C292 C293 10UF 16V

VCC12 VCC12
VCC5 V5P0
VCC2_5 V2P5
VCCVID V2P0
VCC3V V3P3

VCCVID PLANE

Change R254 from 10K to 10

VCC12
VCCVID
R254
10

U22 SC1186
VCC
VID0
VID1
VID2
VID3
VID4
EN
AGND
PGNDL
LDOV
BSTH
BSTL
CS+
CS-
SENSE
DH
DL
PGNDH
LDOS1
GATE1
LDOS2
GATE2
REF
LDOIN

C273 0.1UF

Place CAPs Close to FETs

TH 1.5UH 10% 0.002 OHM 15A
L3

Q9 NDP6030L N-Channel
Q10 NDP6030L N-Channel
DH
DL
GATE2_5
GATE1_5

C261 C262 C263 C264 C265 100UF
C266 0.1UF
C267 0.1UF
C268 C269 C270 C271 C272 1000UF
VCCVID

Place CAPs Close to FETs

VCC2_5
Q11 NDT014L
C274 C275 220UF
2.5V I 1A

C276 220UF
Q12 NDT014L
VCC3V
V1P5
C277 220UF
Place CAPs Close to FETs
C278 C279 220UF
1.5V I 3A

VCC12
Place CAPs Close to FETs
C280 NO LOAD 220UF
LM358 U23A
SC_REF
Q13 NDT014L
R255 42.2 1%
R256 100
V1P8
C281 C282 220UF
1.8V I 1.5A

VOUT	RA1	RB1	
1.5V	18.7	100	
1.8V	42.2	100	Default
2.5V	97.6	100	

PIN OUT
D
G S
NDT014L
SOT-223

1.8V PLANE

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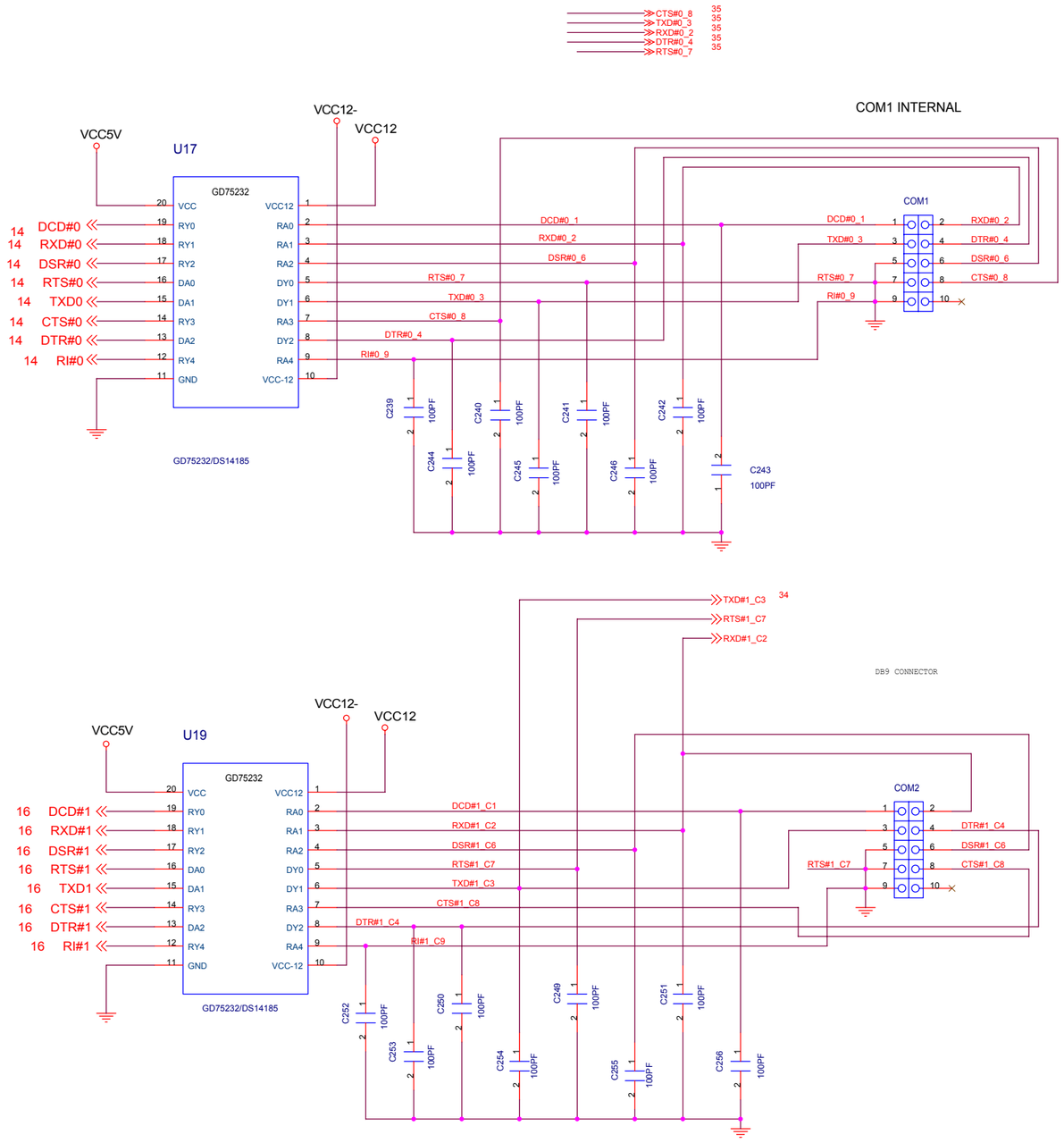

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Title: Serial			
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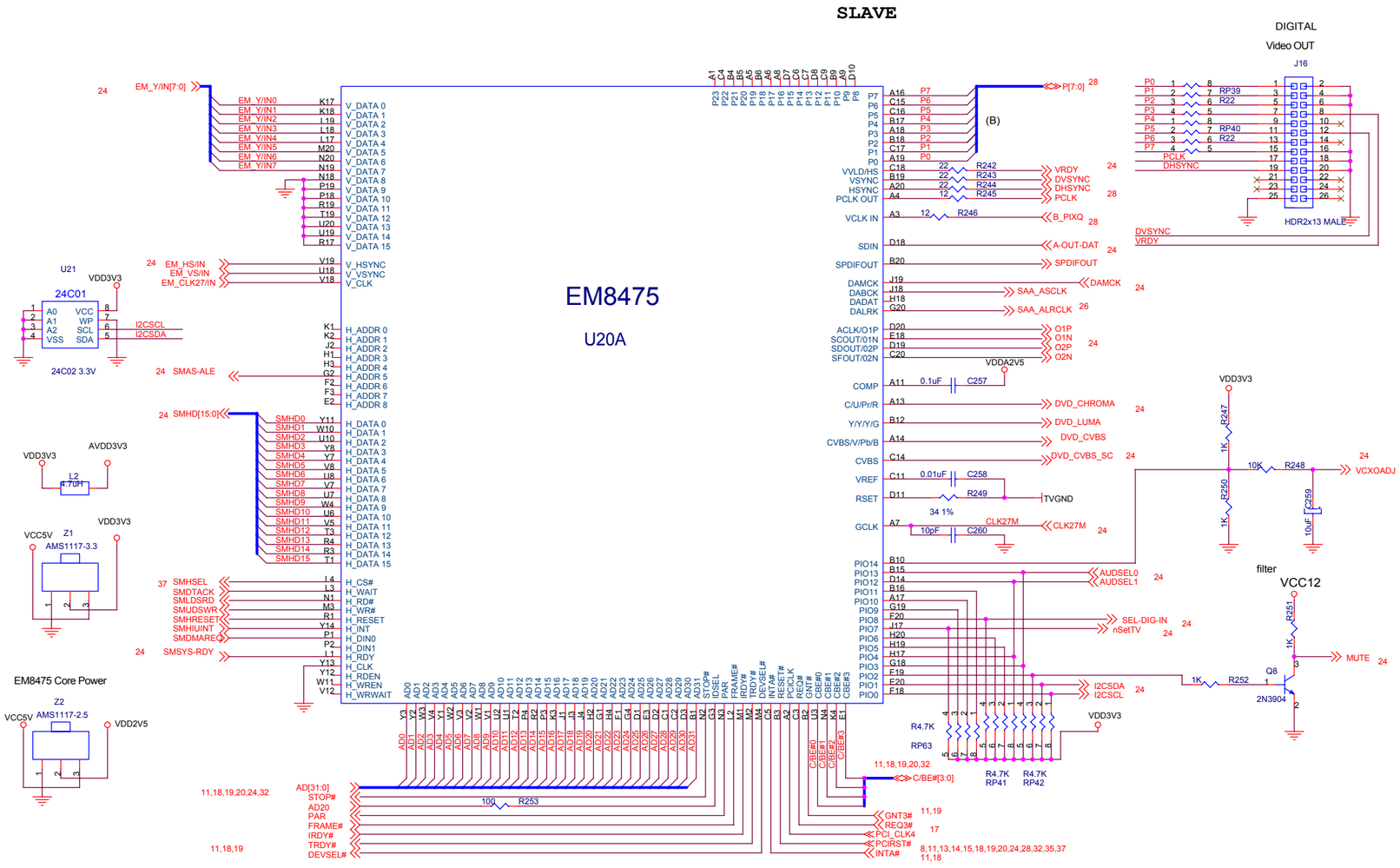
EM8475



Intel® Media Center Reference Platform	
Title	EM8475
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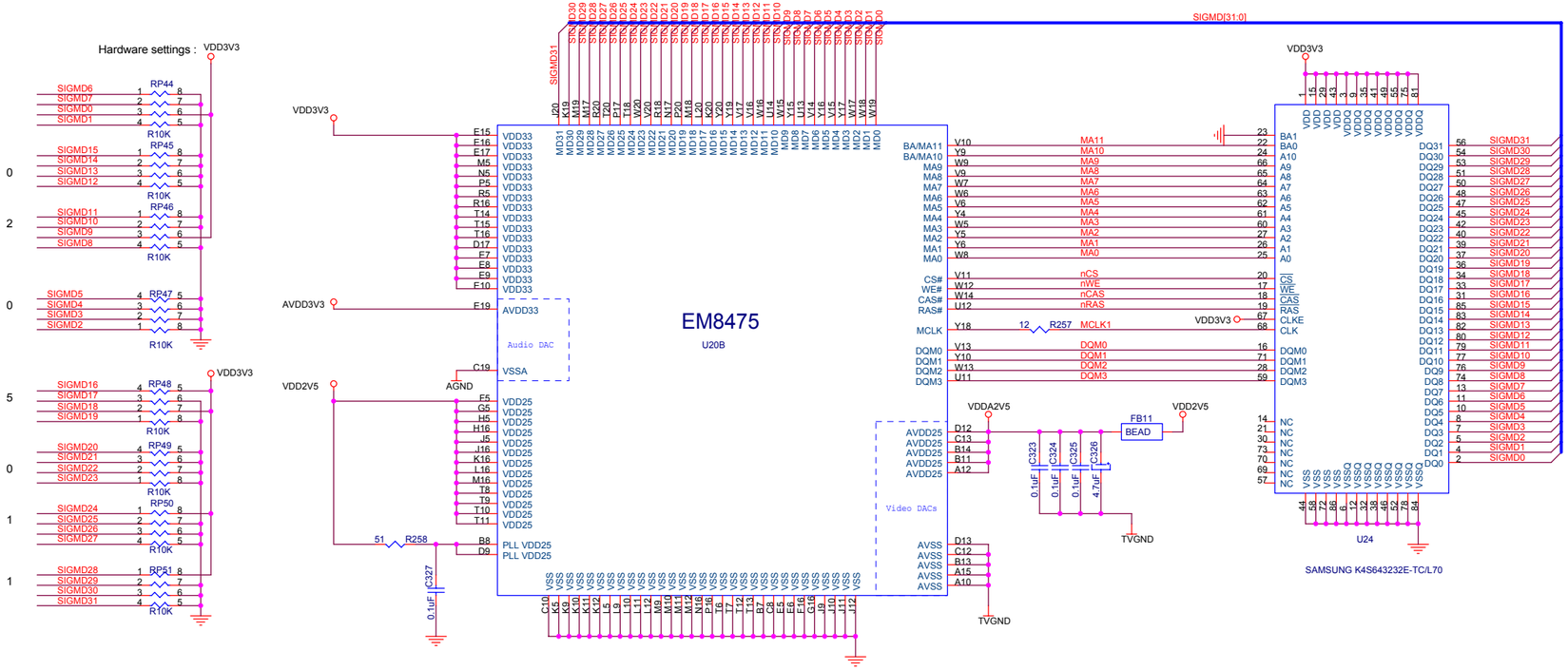
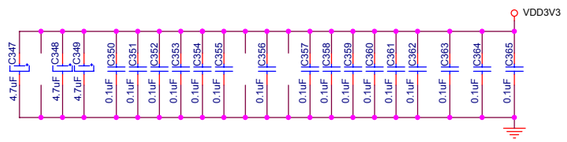
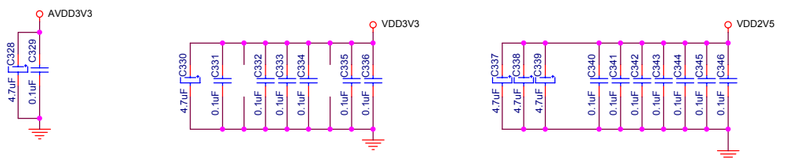
EM8475 & SDRAM







Intel Media Center Reference Platform		
Title: EM8475 & SDRAM		
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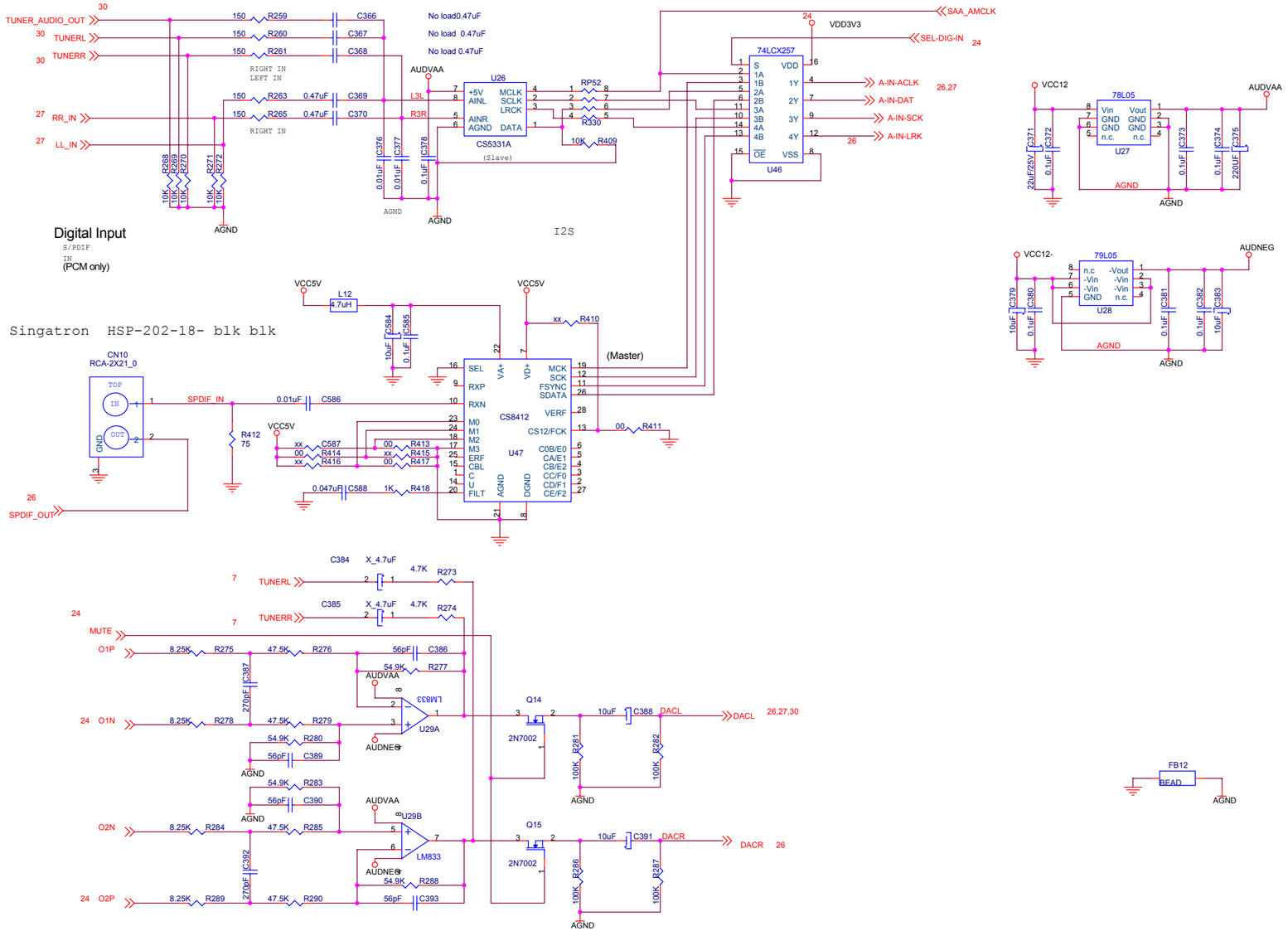
Audio IN/OUT Analog & Digital



Intel® Media Center Reference Platform			
Title: Audio IN/OUT Analog & Digital			
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TV Audio S/PDIF Out & VCXO

CN5
RCA3X1 Video Component
Foxcom JR11030-771
Y Green/Yellow
Pb BLUE
Pr RED
Y_COM FB13 BEAD 3 3T YELLOW
Pb_COM FB14 BEAD 2 2T BLUE
Pr_COM FB16 BEAD 1 1T RED
4 5 6 7 8 TVGND

VCC3V 74LCX08 U45A U45B U45C U45D
VCC5V C575 0.1UF
OPTICAL OUT
CN9 GND VCC VIN OPTICAL
FOXCONN P/N 2F11381-TM1

Digital Output
S/PDIF OUT
PCM / AC-3 / DTS
24 SPDIFOUT 74LCX08 0.1uF C396 220 R293 120 R294 SPDIF_OUT 26

24 AUDSEL0
AUDSEL1
VDD3V3 74LCX08 U30A
FB15 BEAD U32 VDD OUT GND OSC 40MHz
C394 0.1uF C395 22pF
1.5x playback
27MHz x 1.5 = 40MHz
U31 74AC253SC S0 S1 I0a I1a I2a I3a I0b I1b I2b I3b Vcc Za OEa Zb OEb GND
33 R291 33 R292 DAMCK 24

VDD3V3 FB17 BEAD X2 VDD ADJ OUT GND
24 VCXOADJ 33 R295
C397 0.1uF C398 22pF
VCXO 27MHz

26,27 A-IN-ACLK

(default)

AUDSEL0	1	1	0	0
AUDSEL1	1	0	1	0
DAMCK	Tri.	VCXO	Capt.	1.5x

TOP AUDIO VIDEO OUT
CN6
VIDEO IN
RCA3X2
VIDEO YELLOW R OUT IN
R OUT IN
L WHITE OUT IN
L OUT IN
RED OUT IN
AGND
BOTTOM AUDIO VIDEO IN

26 RR_IN FB18 BEAD RIN
26 DACR FB19 BEAD ROUT
LL_IN FB20 BEAD LIN
26,27,30 DACL FB21 BEAD LOUT
TVGNN R298 0 VGND3
R300 0 TVGND
TVGND

VCC5 R296 100 R297 220
R299 75.0 C399 220UF TUNER_VIDEO_IN
Q16 2N3906
C400 47pf TVGND
FB22 BEAD CVBS_O
CVBS_FB_IN BEAD FB23 CVBS_IN
VGND3 27

TV / HDTV OUT

VCC3V RA1 4.7K
VCC5V
U33 PI5V330
24 DVD_CHROMA S1A
28 FS_CHROMA S2A
24 DVD_LUMA S1B
28 FS_LUMA S2B
24 DVD_CVBS S1C
28 FS_CVBS S2C
24 DVD_CVBS_SC S1D
28 CVBS_SYNC S2D
VCC DA DB DC DD IN EN# GND
R_C G_Y B_CVBS CVBS_SYN
24 nSetTV
TVGND
0 = SIGMA DVD
1 = FOCUS
J20 HDR1x2 TVGND

22pF C401 1.8uH L4
22pF C402 1.8uH L5
22pF C403 1.8uH L6
22pF C404 1.8uH L7
C405 330pF C406 330pF C407 330pF C408 330pF
VCC5 R75 RP53 CR10 BAV99 CR11 BAV99 CR12 BAV99 CR13 BAV99
TVGND

Pr_COM BEAD FB24
Y_COM BEAD FB25
Pb_COM
C_OUT_R L_OUT_G
CN7 C1 CGND LGND L1 C2 CGND LGND L2 OUT IN
GND_CHASSIS
BEAD FB26 LUMA_IN 27
VGND1 VGND2
BEAD FB27 CHROMA_IN

DIGITAL GND R301 0 TVGND
DIGITAL GND R302 X_0 VGND

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Title	TV Audio S/PDIF Out & VCXO		
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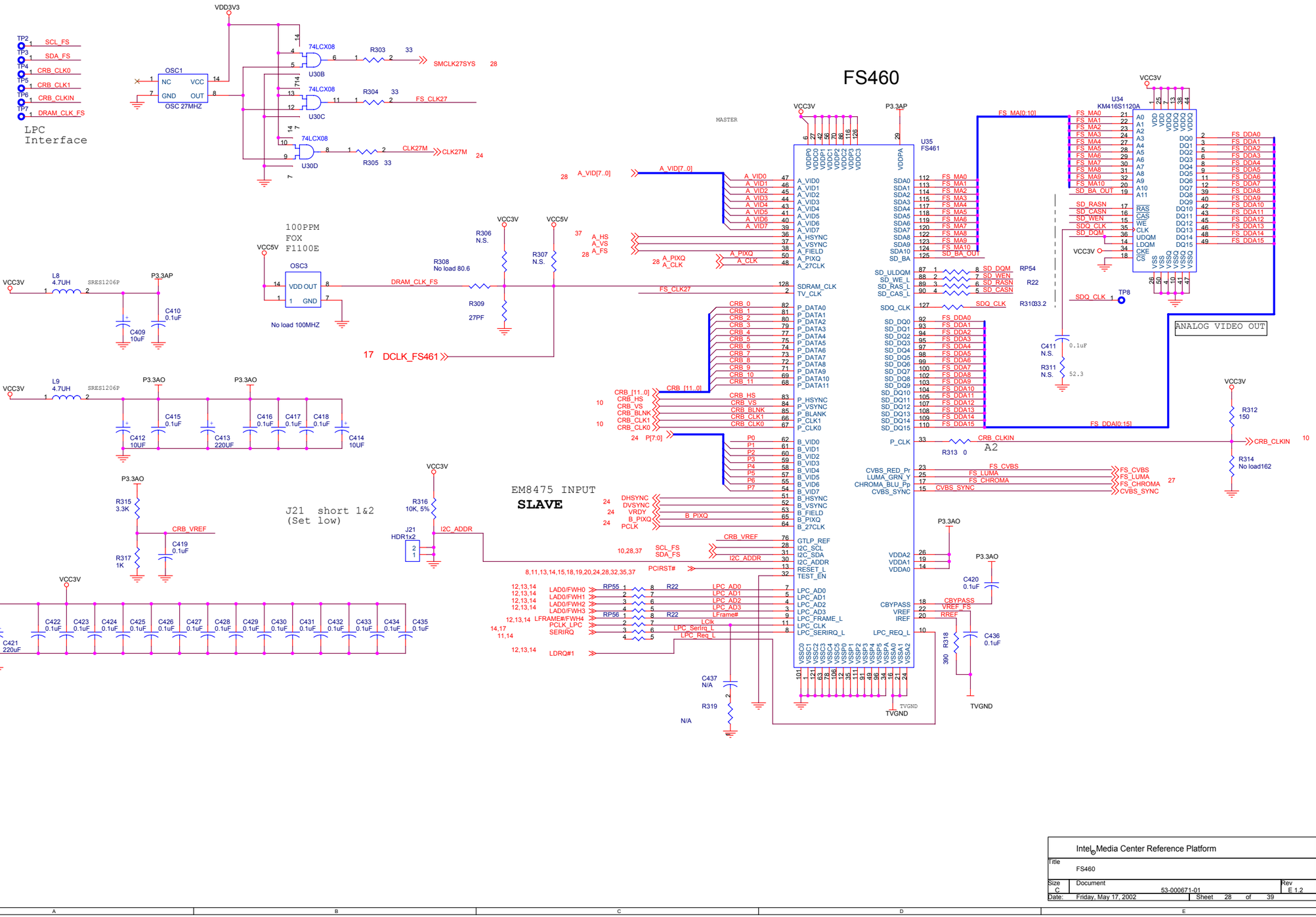
FS460



Intel® Media Center Reference Platform			
Title: FS460			
Size: C	Document: 53-000671-01		Rev: E 1.2
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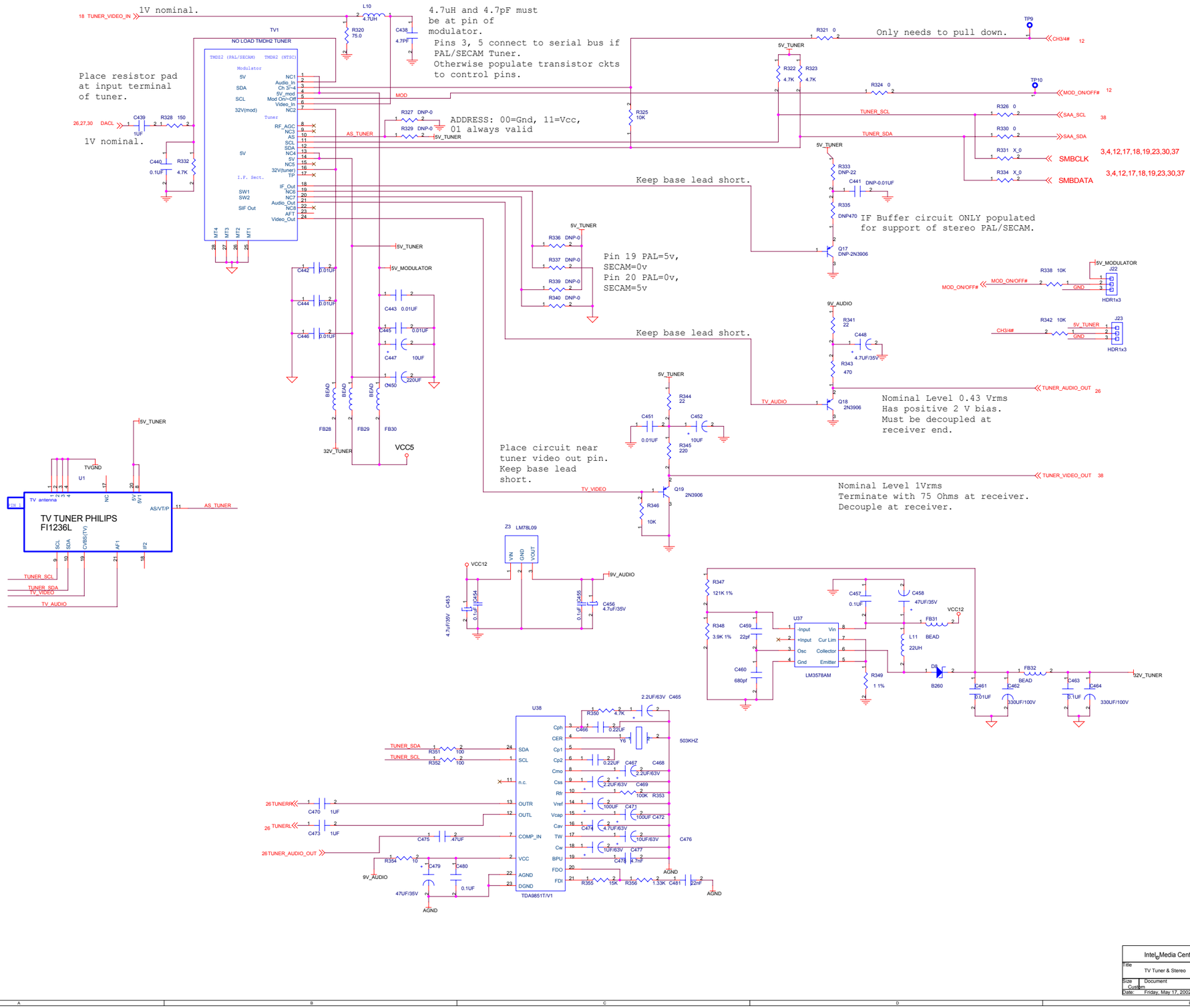
TV Tuner & Stereo



Intel Media Center Reference Platform			
Title: TV Tuner & Stereo			
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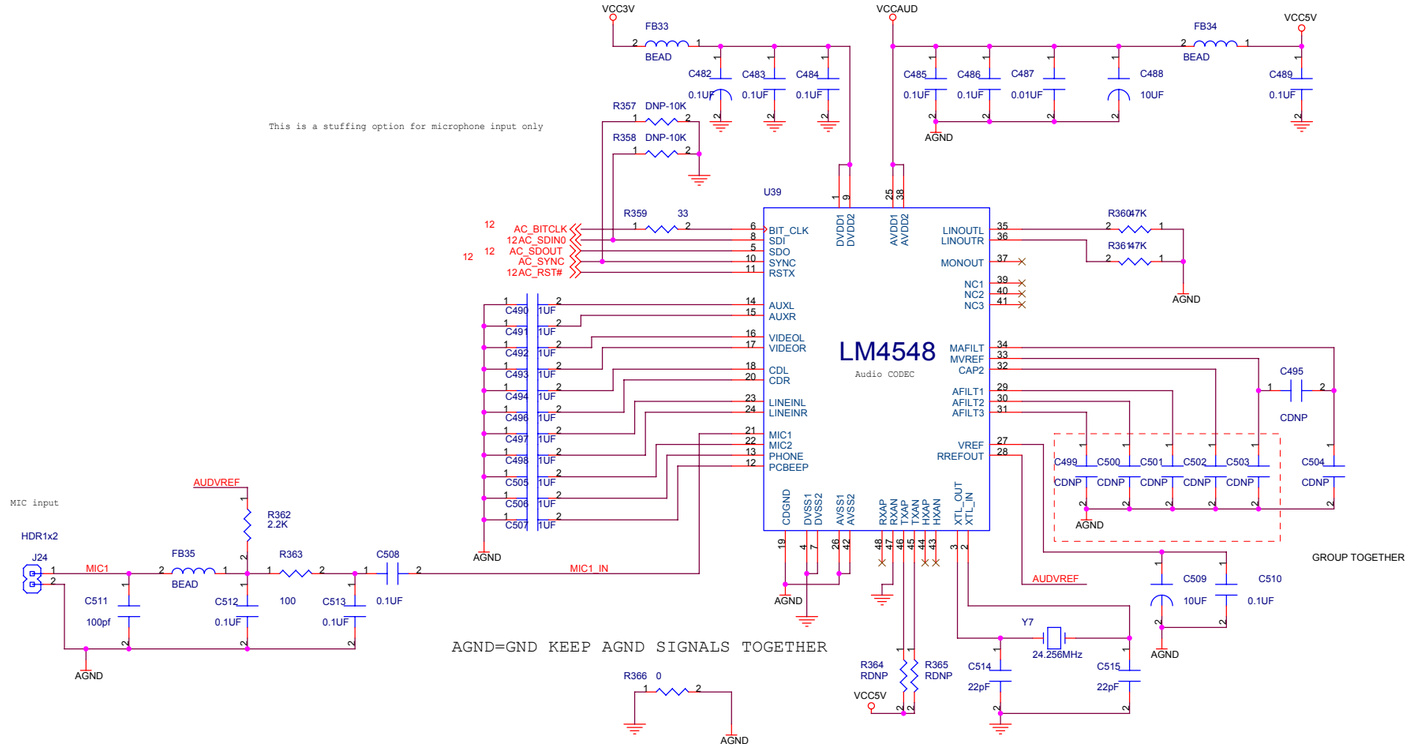
This is a stuffing option for microphone input only



Intel Media Center Reference Platform		
Title: LM4548 Audio Codec		
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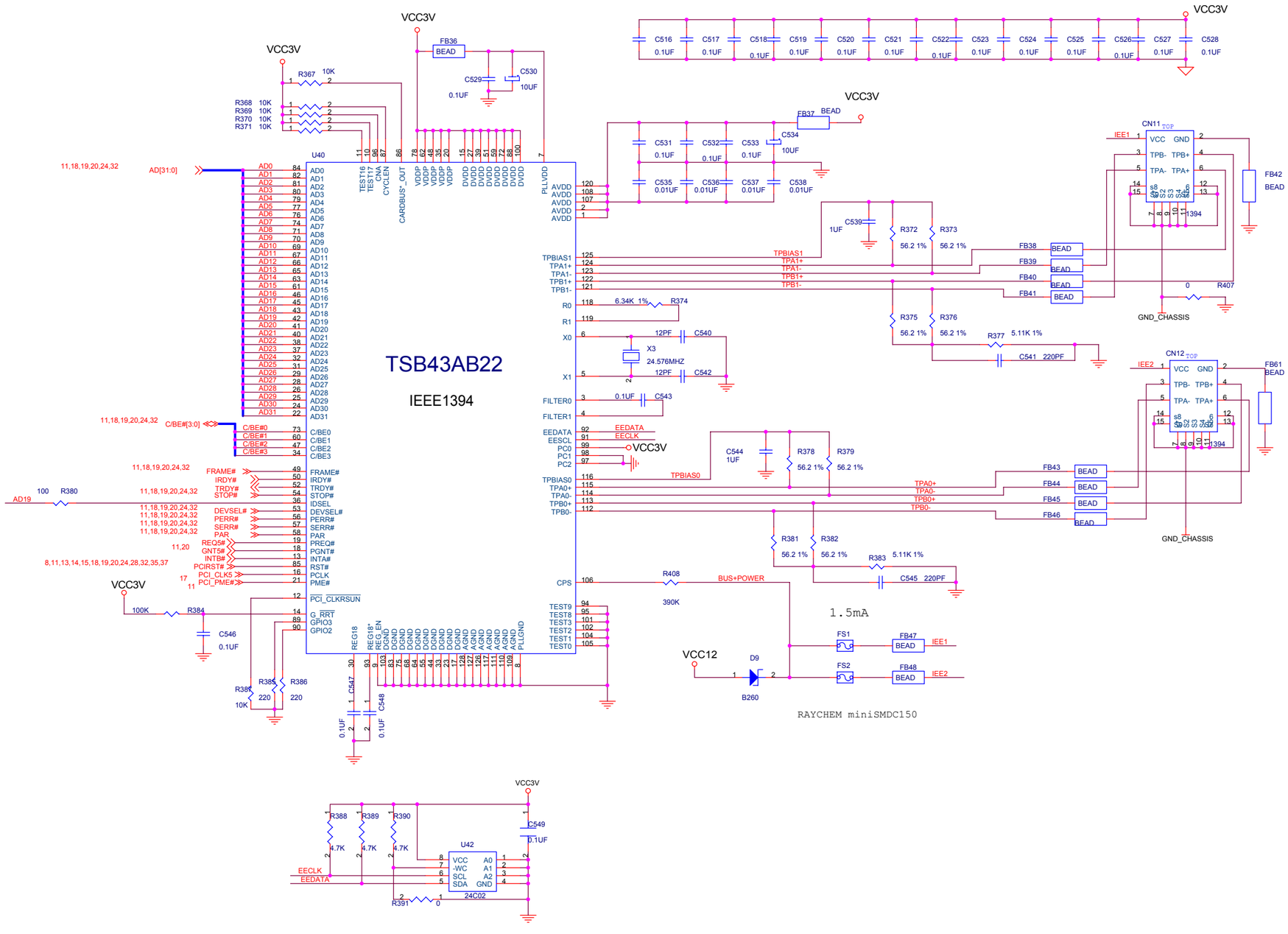
IEEE 1394 TSB43AB22



Intel® Media Center Reference Platform	
Title	IEEE1394 TSB43AB22
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Title: Intentionally Left Blank			
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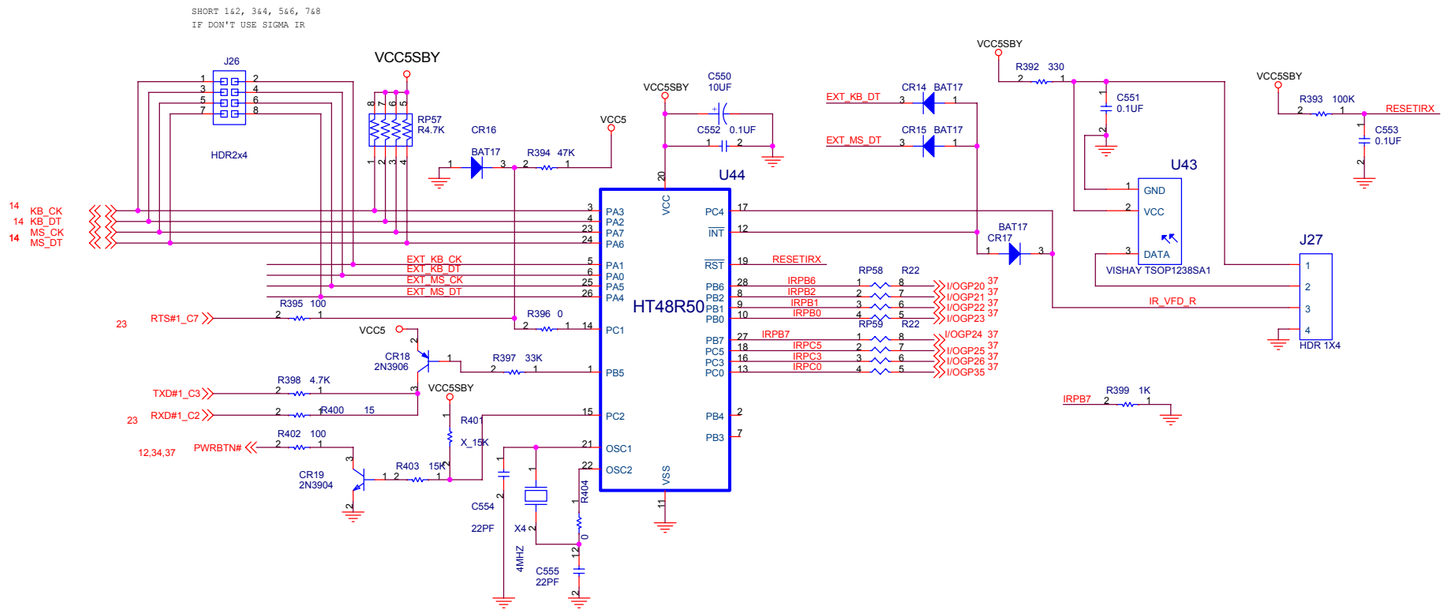
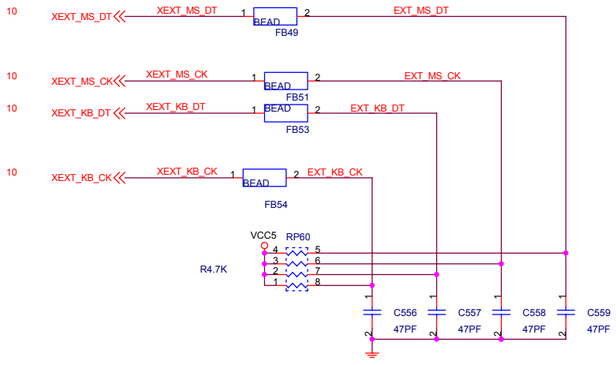
IR Receiver Front I/O





Intel® Media Center Reference Platform		
Title: IR Receiver Front I/O		
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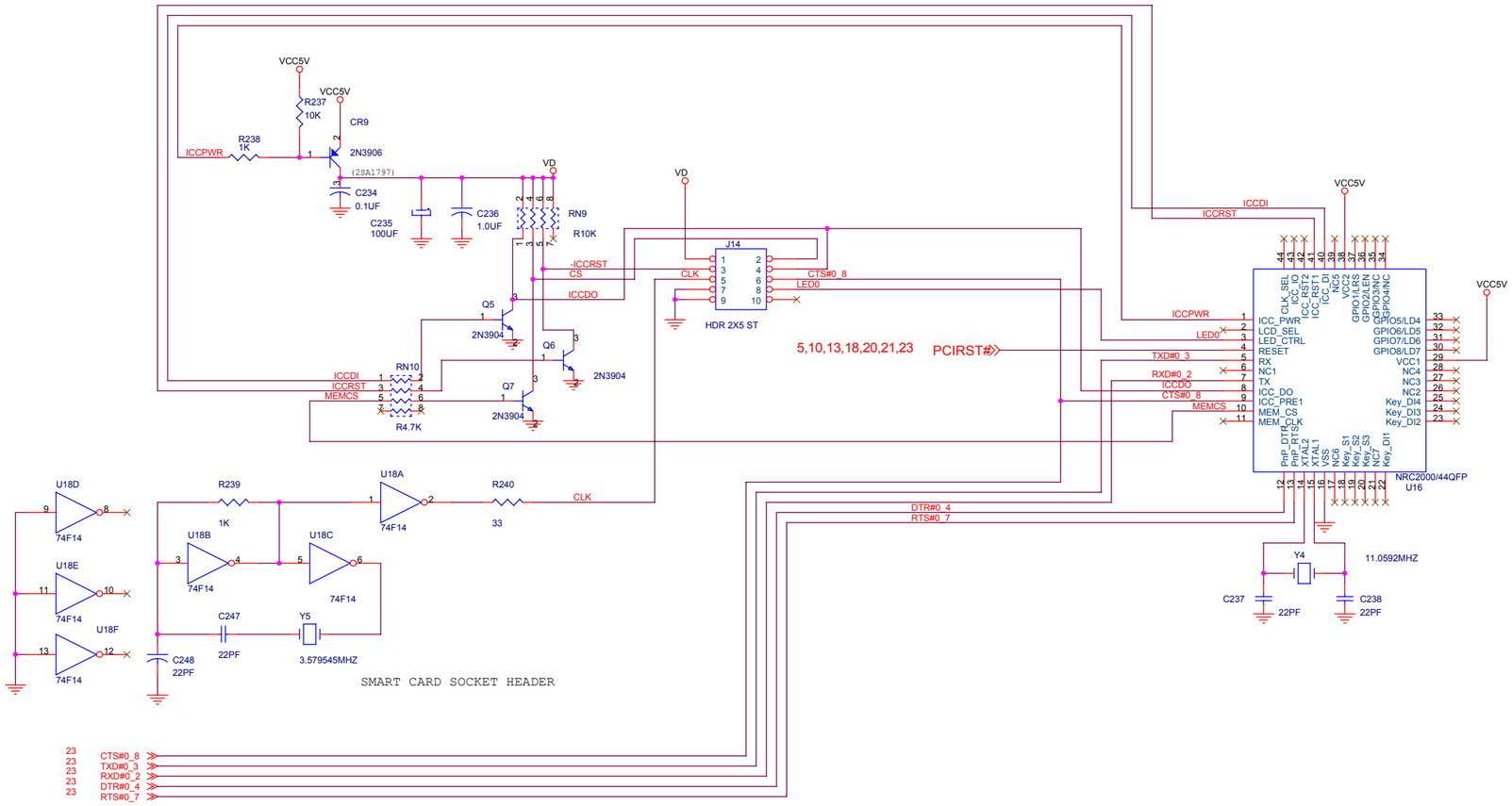
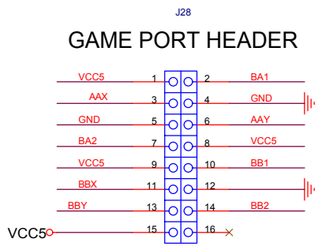
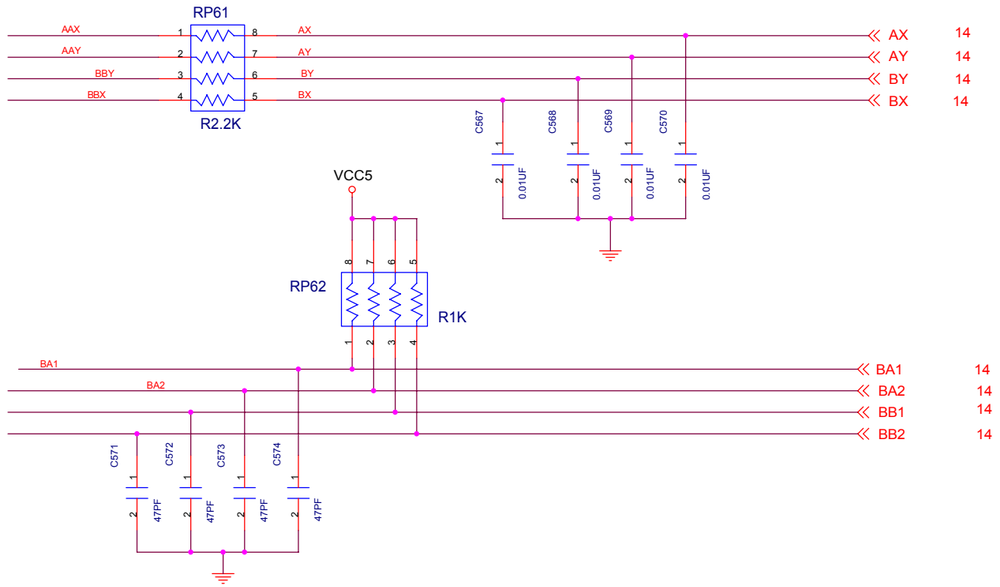
Smart Card


VCC5V
R237
10K
CR9
R238
1K
ICCPWR
2N3906
(2SA1797)
C234
0.1UF
C235
100UF
C236
1.0UF
RN9
R10K
VD
J14
HDR 2X5 ST
-ICCRST
CS
ICCDO
CLK
CTS#0_8
LED0
Q5
2N3904
Q6
2N3904
Q7
2N3904
RN10
R4.7K
ICCDI
ICCRST
MEMCS
5,10,13,18,20,21,23
PCIRST#
TXD#0_3
RXD#0_2
DTR#0_4
RTS#0_7
ICC_PWR
LCD_SEL
LED_CTRL
RESET
RX
NC1
TX
ICC_DO
ICC_PRE1
MEM_CS
MEM_CLK
PnP_DTR
PnP_RTS
XTAL2
XTAL1
VSS
NC6
Key_S1
Key_S2
Key_S3
NC7
Key_DI1
GPIO5/LD4
GPIO6/LD5
GPIO7/LD6
GPIO8/LD7
VCC1
NC4
NC3
NC2
Key_DI4
Key_DI3
Key_DI2
NRC2000/44QFP
U16
Y4
11.0592MHZ
C237
22PF
C238
22PF
U18D
U18E
U18F
U18A
U18B
U18C
74F14
R239
1K
R240
33
C247
22PF
Y5
3.579545MHZ
C248
22PF
SMART CARD SOCKET HEADER

Game Port Header





Intel® Media Center Reference Platform		
Title: Game Port Header		
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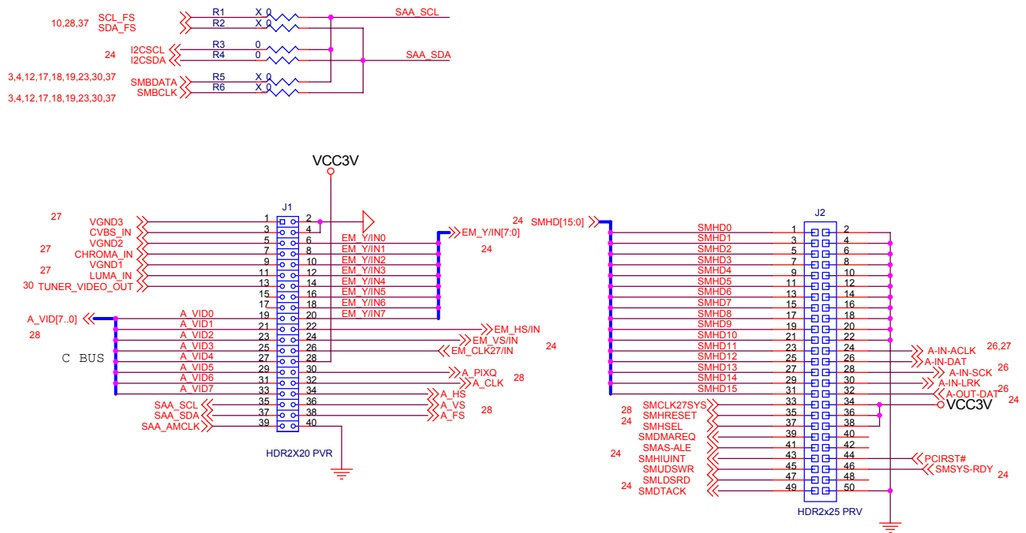
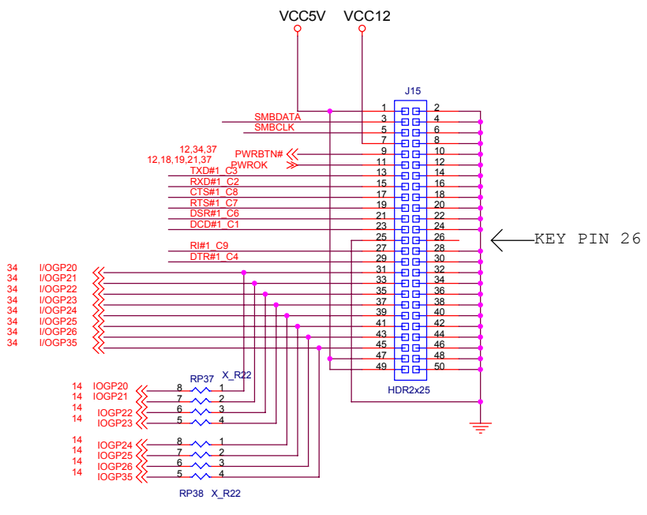
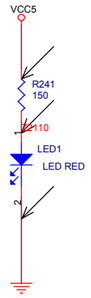
PVR & Front Header







Intel® Media Center Reference Platform		
Title: PVR & Front Header		
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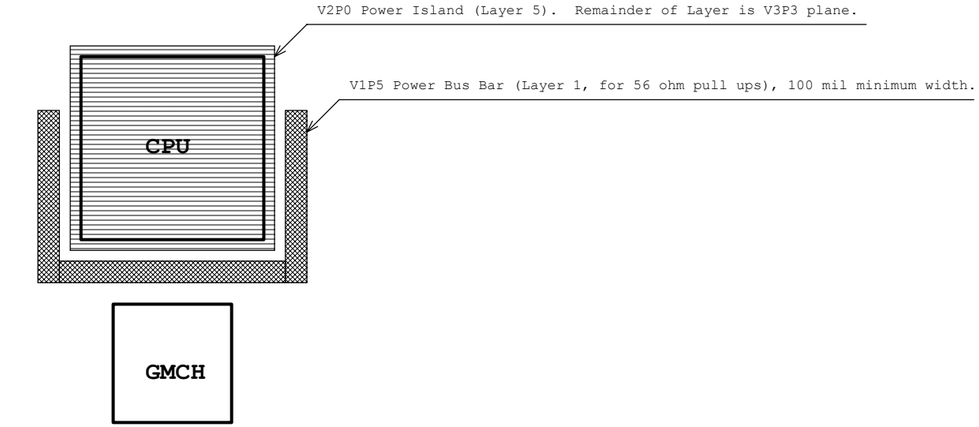
General Placement Requirements

>> Place major components and connectors as shown in the Mechanical drawings.

CPU/GMCH Specific Routing Requirements.

>> Rotate the CPU and GMCH chips so as to minimize the length of the connections between the two, and place as shown in the diagram below:



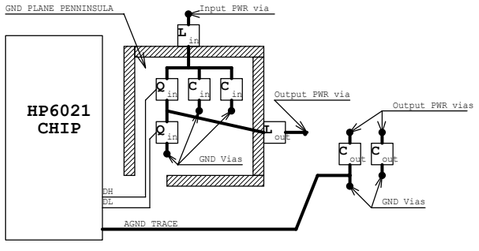
>> The V2P0 power supply must not be layed over the V2P0 power island. The power supply feed to the power island must be the maximum practical width.

>> The V1P5 power supply must not be layed over the V1P5 power island. The power supply feed to the power island must be the maximum practical width.

>> The V2P0 power island depiction above, is approximate, and must be large enough to fully encompass the entire CPU as well as any component that connects to the V2P0 supply.

Power Supply specific Routing Requirements.

>> The diagram below depicts the placement requirements for the SC1164 switching regulator circuits. A GND plane penninsula is used to contain the high current and noisy switching components. All of the bold traces and vias shown have high current and low impedance requirements. These trace widths should be 100 mils minimum. The channel which connects the GND penninsula to the main GND plane must be 500 mils in width.



>> No other signals may be routed underneath the GND plane penninsula.

>> No other power planes may exist underneath the GND plane penninsula.

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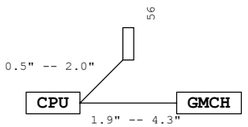
General Board Design Requirements

>> PCB must be routed using six (6) layers, with the following stackup:

Layer 1: Signal, V1P5,V1P8, V2P5, and V5P0 Busses
Layer 2: GND
Layer 3: Signal
Layer 4: Signal
Layer 5: Split Power Plane -- V3P3 Plane, V2P0 Island
Layer 6: Signal

>> Right angle traces must not be used.
>> Vias for decoupling capacitors must be kept as close as possible to the capacitor pad.
>> Trace impedance must be 65 ohms, +/- 10%
>> Total board thickness must be .062".
>> Board material must be FR-4.
>> GND layers must not be split.
>> Top and bottom (outer) layers must be no less than 1/2 oz copper before plating, inner layers must be 1 oz copper.
>> Series terminating resistors must be kept as close to the driving pin as possible.
>> Daisy chain signals going to more that on point, do not use stubs.
>> Unless otherwise noted, all signal traces must be between 5 and 6 mil width.
>> Unless otherwise noted, minimum space between traces is 15 mils, including adjacent layers.
>> Specific routing reqirements are included throughout schematic sheets.
>> One registration target must be included on each corner of the board.

CPU Routing Requirements



>> Route all GTL traces between CPU and GMCH as shown in the diagram to the right.
>> Route all traces between CPU and GMCH on a layer adjacent to a ground plane (preferably bottom layer), without layer changes.
>> All traces between CPU and GMCH should differ in length by no more than 1000 mils.
>> Minimum space between traces is 15 mils (unless otherwise noted), this includes adjacent signal layers.
>> Minimum space between traces may be reduced to 5 mils when breaking out of a footprint. The total length of trace routed using 5 mil spacing must be less than 250 mils.
>> The following signals require 25 mil spacing from other traces, including adjacent layers.

HA#[31:3], HD#[63:0], BREQ#0, ADS#, BNR#, BPRI#, HLOCK#, DEFER#, HTRDY#, DBSY#, DRDY#, HIT#, HITM#, A20M#, FLASH#, IGNNE#, INIT#, INTR, NMI, PWR_OK_2P5, SMI#, CPUSLP#, STPCLK#, 100/66#, FERR#, HRESET#, HREQ#[4:0], RS#[2:0], THERMD[P:N], CPU_GTL_REF[7:0], PLL[2:1], (TCK,TMS,TDI, TDO, TRST#, PRDY#, PREQ#).

>> Route THRMDP and THRMDN close together as a pair (no more than 250 mil difference in length), on same layer, in parallel, and 25 mils min from any other trace.
>> Route CPU_GTLREF using 25 mil minimum width trace, and separate from all other traces by 25 mils minimum.
>> Route PLL[2:1] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum.

Clock Specific Routing Requirements

>> A clock trace must not alternate layers.
>> A clock trace must be separated by a minimum of 25 mils from any other trace, including serpentines, 11 mils is OK when going betwen pins or balls.
>> The CPU clock length must be between 1" and 9", and 460 mils shorter than the GMCH clock. The GMCH_3V66 clock and ICH_3V66 clock must be matched in length. All PCI clocks must be matched in length, except for the PMC clock which must be 2" shorter than all other PCI clocks.
>> SDRAM_CLK[1:0] must be matched in length, and between 1" and 3" in length.
>> DCKL_WR, from the SDRAM clock driver to the GMCH, must be between 3.5" and 5.5" in length, and 2.5" longer than SDRAM_CLK[1:0].

IDE Specific Routing Requirements

>> Place IDE conector within 8" of ICH.

Power Supply Specific Routing Requirements

>> All unrelated signals and power planes must be kept away from the switching circuits.
>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.
>> See the Power Supply schematic sheet for complete restrictions.

Memory Bus Specific Routing Requirements

>> Minimum trace width is 5 mils.
>> Minimum space between traces is 10 mils, this includes adjacent signal layers.
>> Minimum space between memory traces and other types of traces is 25 mils, this includes adjacent signal layers.
>> Memory address, data, and control lines must be routed as separate groups and treated as different signal types.
>> The MD, DQMA, CSA#, SRAS#, SCAS#, WE_A#, and MA signals (between GMCH and SODIMM) must be between 1" and 3" in length, matched to within 600 mils.

Memory Bus GROUPS -- SO-DIMM Names

>> Address Signals: MAA[13:0]
>> Data Signals: MD#[63:0]
>> Control Signals:

SMBDATA, SMBCLK, CSA[1:0]#, WE_A#, SCAS#, SRAS#

PCI Bus Specific Routing Requirements

>> PCI bus max length must be less than 6".

PCI Bus GROUPS

>> Address/Data Signals: AD[31:0]
>> Control Signals:

C/BE[3:0]#, REQ[5:1]#, GNT[5:1]#, INT[A:D]#, PCIRST#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PERR#, PAR, LOCK#

HUB Bus GROUPS

>> Address/Data Signals: HL[10:0]
>> Control Signals: HLSTB,HLSTB# (differential strobe pair).
>> HL[10:0] should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. The maximum trace length for the hub interface data signals is 7". These signals should each be matched within .1"” of the HLSTB and HLSTB# signals.

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